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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	501.35437VX1	Total Pages	
First Named Inventor or Application Identifier	YOSHIDA et al.		
Express Mail Label No.			

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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1. [x] Fee: $760.00

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2. [x] Specification [Total Pages 54]
3. [x] Drawing(s) *(35 USC 113)* [Total Sheets 49]
4. Oath or Declaration [Total Pages 2]
   a. [ ] Newly executed (original or copy)
   b. [x] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* *[Note Box 5 below]*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [x] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [x] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [x] Preliminary Amendment
13. [x] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other: .....

17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information:*
[ ] Continuation [x] Divisional [ ] Continuation-in-part (CIP) of prior application No: 08 / 865,864

18. CORRESPONDENCE ADDRESS

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11. SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

NAME	Gregory E. Montone		
SIGNATURE			
DATE	October 13, 1999	REG. NO.	28,141

ANTONELLI, TERRY, STOUT & KRAUS, LLP
SUITE 1800
1300 NORTH SEVENTEENTH STREET
ARLINGTON, VIRGINIA 22209

TELEPHONE
(703) 312-6600
FACSIMILE
(703) 312-6666
E-MAIL
email@antonelli.com

501.35437VX1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	M. YOSHIDA et al.
Serial No.:	08/865,864
Filed:	May 30, 1997
For:	SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND PROCESS FOR MANUFACTURING THE SAME
Group:	2812
Examiner:	J. Hack

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

October 13, 1999

Sir:

Prior to examination, please amend the above-identified application as follows:

IN THE SPECIFICATION

Page 1, at the top of the page, insert the following:

-- CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional of application Serial No. 08/865,864, filed May 30, 1997, the entire disclosure of which is hereby incorporated by reference. --

Page 1, line 13, delete "a" and insert --the--;

line 16, delete "Summary" and insert --Background--;

line 18, delete "is" and insert --has--, delete "by", delete "of a" and insert --in that the--;

line 19, after "cost" insert --of manufacture has been--, delete "the" (first occurrence) and insert --an--, after "of" insert --manufacturing--;

line 20, delete "because its manufacture process is" and insert --as the manufacturing process becomes more--;

line 21, delete "more as its" and insert --with increases in--, delete "grow";

line 22, delete "higher";

line 23, delete "depositing", after "films" (second occurrence) insert --deposited--;

line 25, delete "is" and insert --has--.

Page 2, between lines 4 and 5, insert the heading: --Summary of the Invention--;

line 19, delete "prove the manufacture" and insert --improve the manufacturing--.

Page 3, line 10, after "of" (second occurrence) insert --the--;

line 21, after "of" (second occurrence) insert --the--.

Page 6, line 2, delete "sections" and insert --section views--;

line 3, after "show" insert --respective steps of--;

line 5, delete "of" (first occurrence) and insert --representing an--;

line 7, after "a" (first occurrence) insert --cross--;

line 8, delete "show" and insert --shows the steps of--;

line 10, delete "of" (first occurrence) and insert --representing an--;

line 11, delete "sections" and insert --section views--;

line 12, after "show" insert --respective steps of--;

line 14, delete "of" (first occurrence) and insert --representing an--;

line 16, delete "sections" and insert --section views--;

line 17, after "show" insert --respective steps of--;

line 19, delete "of" (first occurrence) and insert --representing an--;

line 21, delete "sections" and insert --section views--;

line 22, after "show" insert --respective steps of--;

line 24, delete "of" (first occurrence) and insert --representing an--.

Page 7, line 1, delete "sections" and insert --section views--;

line 2, after "show" insert --respective steps of--;

line 4, delete "of" (first occurrence) and insert --representing an--;

line 6, delete "sections" and insert --section views--;

line 7, after "show" insert --respective steps of--;

line 9, delete "of" and insert --representing an--;

line 11, delete "showing" and insert --of--;

line 13, delete "of" (first occurrence) and insert --representing an--;

line 14, delete "sections" and insert --section views--;

line 15, after "show" insert --respective steps of--;

line 17, delete "of" (first occurrence) and insert --representing an--;

line 23, after "the" (second occurrence) insert --various--;

line 24, after "embodiments" insert --,--.

Page 8, line 6, after "," insert --and--.

Page 9, line 1, after "1" insert --,--;

line 3, after "circuit" insert --,--;

line 6, after "1" insert --,--;

line 7, after "circuit" insert --,--.

Page 10, line 9, delete "the" and insert --a--;

line 11, delete "coped" and insert --doped--;

line 12, delete "the" and insert --a--;

line 15, delete "the" and insert --a--;

line 17, delete "the" (second occurrence) and insert --a--.

Page 11, line 7, delete "the" (first occurrence) and insert --a--;

line 10, delete "the" and insert --a--;

line 16, delete "by" and insert --using--;

line 17, delete ","; same line 17, delete "by" (second occurrence) and insert --using--;

line 22, delete "the".

Page 13, line 11, delete "by" and insert --using--;

line 15, delete "by";

line 16, delete "the" and insert --a--.

Page 17, line 24, delete "the" (first occurrence) and insert --a--.

Page 18, line 12, after "method" insert --such--; same line 12, after "as" insert --used--.

Page 19, line 1, delete "the" (first occurrence) and insert --a--;

line 18, delete "the" and insert --a--.

Page 20, line 5, delete "the" and insert --a--.

Page 21, line 1, delete "the" and insert --a--;

line 5, after "after" insert --formation of--;

line 8, delete "have been formed";

line 17, after "all" insert --of--.

Page 23, line 1, delete "the" (second occurrence);

line 13, delete "the" and insert --a--;

line 14, after "of" insert --the--.

Page 24, line 13, delete "the" and insert --a--;

line 17, delete "the" (second occurrence) and insert --a--.

Page 27, line 3, after "that" insert --a--;

line 11, delete "by the manufacture" and insert --employing the manufacturing--;

line 18, delete "by" and insert --using--;

line 20, delete "by";

line 21, delete "the" (first occurrence) and insert --a--.

Page 29, line 2, delete "a";

line 14, delete "the" (second occurrence) and insert --a--.

Page 31, line 2, delete "the" and insert --a--;

line 3, delete "matters" and insert --matter--;

line 14, delete "the";

line 18, delete "the" and insert --a--; same line 18, delete "of" and insert --to occur in--.

Page 32, line 8, delete "the" (first occurrence) and insert --a--, delete "of" and insert --to occur in--;

line 23, delete "the" and insert --a--.

Page 33, line 12, delete "the" (both occurrences);

line 20, after "off" insert --,--; same line 20, after "but" insert --is--.

Page 34, line 13, delete "the" (first occurrence) and insert --a--;

line 24, delete "at the" and insert --in a--;

line 25, delete "manufacture" and insert --manufacturing--.

Page 36, line 13, delete "the" and insert --a--.

Page 38, line 19, delete "the" and insert --an--;

line 20, delete "the" and insert --a--;

line 21, after "ratio" insert --with respect--.

Page 39, line 4, delete "the" and insert --a--.

Page 40, line 23, delete "the" (first occurrence) and insert --a--;

line 25, delete "the" (first occurrence) and insert --an--.

Page 42, line 8, delete "the" (first occurrence) and insert --a--.

Page 44, line 18, delete "the" and insert --a--.

Page 45, line 1, delete "ration" and insert --region--;

line 10, delete "of" (second occurrence).

Page 47, line 3, delete "at the"; same line 3, after "totally" insert --at--;

line 17, delete "manufacture" and insert --manufacturing--.

Page 48, line 1, delete "is" and insert --are--;

line 25, delete "the" (second occurrence) and insert --a--.

Page 49, line 2, delete "the" (second occurrence) and insert --a--;

line 3, delete "by"; same line 3, after "totally" insert --by--;

line 7, delete "the" and insert --a--;

line 14, delete "taking the cases of" and insert --with reference to various--; same line 14, delete "it" and insert --the invention--;

line 18, delete "representatives of" and insert --representative--;

line 19, delete "the aspect" and insert --aspects--;

line 21, delete "manufacture" and insert --manufacturing--.

Page 50, lines 2, 8 and 12, delete "manufacture" and insert --manufacturing--.

REMARKS

The specification has been amended to correct errors of a typographical and grammatical nature.

Entry of the preliminary amendments and examination of the application is respectfully requested.

Also new claims are presented for examination in this divisional case.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (501.35437VX1), and please credit any excess fees to said deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

Gregory E. Montone
Registration No. 28,141

GEM/vlc
(703) 312-6600

SPECIFICATION

TITLE OF THE INVENTION

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND PROCESS FOR MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a technique for manufacturing a semiconductor integrated circuit device having MISFETs (Metal Insulator Semiconductor Field Effect Transistors) and, more particularly, to a technique which is effective if applied to a manufacture of a semiconductor integrated circuit device having a DRAM (Dynamic Random Access Memory).

Summary of the Invention

The LSI, represented by a large capacity DRAM of recent years, is encountered by a serious problem of a high cost raised by the increase in the number of steps, because its manufacture process is complicated more as its integration, speed and function grow higher. In accordance with this, the number of depositing insulating films and conductive films over a semiconductor substrate at a temperature of 700 to 900°C is increased to make it difficult to achieve a

high performance for the MISFETs by realizing a shallow junction. Moreover, the increase in the wiring resistance resulting from the miniaturization raises an obstruction to the speedup.

An object of the present invention is to provide a technique capable of reducing the number of heat treatment steps in a process for manufacturing a semiconductor integrated circuit device having MISFETs.

Another object of the present invention is to provide a technique capable of simplifying the process for manufacturing a semiconductor integrated circuit device having MISFETs.

Another object of the present invention is to provide a technique capable of lowering the wiring resistance of a semiconductor integrated circuit device having MISFETs.

Another object of the present invention is to prove the manufacture yield of a semiconductor integrated circuit device having DRAMs.

Another object of the present invention is to improve the electrical characteristics of a semiconductor integrated circuit device having DRAMs.

The aforementioned and other objects and novel features of the present invention will become apparent

from the following description to be made with reference to the accompanying drawings.

Representatives of the aspects of the invention, as disclosed herein, will be briefly described in the following.

By a process for manufacturing a semiconductor integrated circuit device of the present invention, all conductive films to be deposited over a semiconductor substrate are deposited at a temperature of 500°C or lower at a step after formation of MISFETs.

By a process for manufacturing a semiconductor integrated circuit device of the present invention, all conductive films to be deposited over a semiconductor substrate are made of a metal or its compound.

By a process for manufacturing a semiconductor integrated circuit device of the present invention, all insulating films to be deposited over a semiconductor substrate are deposited at a temperature of 500°C or lower at a step after formation of MISFETs.

By the present invention, there is provided a semiconductor integrated circuit device comprising:

(a) a semiconductor substrate having a major

surface;

(b) a first semiconductor region formed in the major surface of said semiconductor substrate;

(c) a first insulating film formed over the major surface of said semiconductor substrate and having a first opening for exposing a portion of said first semiconductor region to the outside;

(d) a first conductor layer made of a polysilicon film formed in said first opening;

(e) a second insulating film positioned over said first insulating film and having a second opening for exposing a portion of said first conductor layer to the outside; and

(f) a second conductor layer formed in said second opening,

wherein a silicide layer is formed at the interface between said first conductor layer and said second conductor layer.

According to the present invention, there is provided a process for manufacturing a semiconductor integrated circuit device comprising:

(a) the step of forming a first semiconductor region in the major surface of a semiconductor substrate;

(b) the step of depositing a first insulating

film over the major surface of said semiconductor substrate;

(c) the step of forming a first opening in said first insulating film in such a way as to expose a portion of said first semiconductor region to the outside;

(d) the step of forming a first conductor layer made of a poly-silicon film selectively in said first opening;

(e) the step of forming a silicide film of a refractory metal layer selectively only over said first conductor layer by depositing said refractory metal film over said first conductor layer and said first insulating film and by subjecting the same to a heat treatment;

(f) the step of removing said refractory metal film over said first insulating film while leaving the silicide film of said refractory metal layer;

(g) the step of depositing a second insulating film over said first insulating film to form a second opening for exposing a portion of the silicide film of said refractory metal layer to the outside; and

(h) the step of forming a second conductor layer in said second opening.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1 to 16 are sections of an essential portion of a semiconductor substrate and show a process for manufacturing a semiconductor integrated circuit device of Embodiment 1 of the present invention;

Fig. 17 is a section of an essential portion of a semiconductor substrate and show a process for manufacturing a semiconductor integrated circuit device of Embodiment 2 of the present invention;

Figs. 18 to 22 are sections of an essential portion of a semiconductor substrate and show a process for manufacturing a semiconductor integrated circuit device of Embodiment 3 of the present invention;

Figs. 23 to 33 are sections of an essential portion of a semiconductor substrate and show a process for manufacturing a semiconductor integrated circuit device of Embodiment 4 of the present invention;

Figs. 34 to 37 are sections of an essential portion of a semiconductor substrate and show a process for manufacturing a semiconductor integrated circuit device of Embodiment 5 of the present invention;

Figs. 38 to 47 are sections of an essential portion of a semiconductor substrate and show a process for manufacturing a semiconductor integrated circuit device of Embodiment 6 of the present invention;

Figs. 48 to 52 are sections of an essential portion of a semiconductor substrate and show a process for manufacturing a semiconductor integrated circuit device of Embodiment 7 of the present invention;

Figs. 53 and 54 are flow charts showing the semiconductor integrated circuit device manufacturing process of Embodiment 7 of the present invention; and

Figs. 55 to 58 are sections of an essential portion of a semiconductor substrate and show a process for manufacturing a semiconductor integrated circuit device of Embodiment 8 of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of the present invention will be described in detail with reference to the accompanying drawings. Throughout the drawings for explaining the embodiments the parts or portions having the same functions are designated by the same reference

numerals, and their repeated description will be omitted.

(Embodiment 1)

The present embodiment is applied to a process for manufacturing a DRAM having memory cells of stacked capacitor structure, in which information storing capacitive elements (capacitors) are arranged over memory cell selecting MISFETs.

For manufacturing this DRAM, first of all, there is prepared a semiconductor substrate 1 which is made of a p^--type single crystal silicon having a specific resistance of about 10 Ω·cm, as shown in Fig. 1. The surface of the semiconductor substrate 1 is oxidized to form a thin silicon oxide film 43, and a silicon nitride film 44 is deposited over the silicon oxide film 43 by a CVD method. This silicon nitride film 44 is etched by using a photoresist as a mask to remove the silicon nitride film 44 from an element isolating region.

Next, as shown in Fig. 2, the semiconductor substrate 1 is annealed at a temperature of about 1,000°C by using the silicon nitride film 44 as a mask, to form a field oxide film 2 having a thickness of about 400 nm.

Next, the silicon nitride film 44 is removed, and

the semiconductor substrate 1 at the regions to form a memory array and to form n-channel MISFETs of a peripheral circuit is doped with ions of a p-type impurity (boron (B)), as shown in Fig. 3, to form a p-type well 3. Moreover, the semiconductor substrate 1 at the region to form p-channel MISFETs of a peripheral circuit is doped with ions of an n-type impurity (phosphor (P)) to form an n-type well 4. Subsequently, the p-type well 3 is doped through the field oxide film 2 with boron (B) ions of a p-type impurity to form a p-channel stopper layer 5 below the field oxide film 2, and the n-type well 4 is doped through the field oxide film 2 with phosphor (P) ions of an n-type impurity to form an n-type channel stopper layer 6 below the field oxide film 2. After this, the surfaces of the individual active regions of the p-type well 3 and the n-type well 4, enclosed by the field oxide film 2, are thermally oxidized at a temperature of about 800°C to form a gate oxide film 7 having a thickness of about 8 nm.

Next, as shown in Fig. 4, there are formed gate electrodes 8A (word lines WL) for the memory cell selecting MISFETs, gate electrodes 8B of the n-channel MISFETs of the peripheral circuit, and gate electrodes 8C of the p-channel MISFETs. These gate electrodes 8A

(word lines WL) and the gate electrodes 8B and 8C are simultaneously formed by depositing a tungsten (W) film having a thickness of about 150 nm at a filming temperature of about 475°C over the semiconductor substrate 1 by a CVD method, by depositing a silicon nitride film 9 having a thickness of about 250 nm at a filming temperature of about 360°C over the W film by a plasma CVD method, and by patterning those films by an etching method using a photoresist as the mask.

Next, as shown in Fig. 5, the p-type well 3 is coped with ions of an n-type impurity such as phosphor (P) or arsenic (As) by using the (not-shown) photo-resist mask for exposing the NMOS forming region to the outside, and the n-type well 4 is doped with boron (8) ions of a p-type impurity by using the (not-shown) photoresist mask for exposing the PMOS forming region to the outside. By the subsequent annealing step, the n-type impurity (P) forms n-type semiconductor regions 11 (a source region and a drain region) of the memory cell selecting MISFETs and n^--type semiconductor region of the n-channel MISFETs of the peripheral circuit in self-alignment with the gate electrodes 8A and 8B, and the p-type impurity (B) forms p^--type semiconductor region 14 of the p-channel MISFETs of the peripheral circuit in self-alignment with the gate electrodes 8C.

Next, as shown in Fig. 6, side wall spacers 10 are formed at the individual side walls of the gate electrode 8A (word lines WL) and gate electrodes 8B and 8C. After this, the p-type well 3 of the peripheral circuit is doped with ions of an n-type impurity such as arsenic (As) or phosphor (P) by using the (not-shown) photoresist mask covering the memory array region and the PMOS forming region of the peripheral circuit, and the n-type well 4 is doped with boron (B) ions of a p-type impurity by using the (not-shown) photoresist mask covering the memory array region and the NMOS forming region of the peripheral circuit. The side wall spacers 10 are formed by depositing a silicon nitride film having a thickness of about 100 nm at a filming temperature of about 360°C over the semiconductor substrate 1 by a plasma CVD method, and by working the silicon nitride film by an anisotropic etching method.

Next, by annealing the semiconductor substrate 1 in a nitrogen atmosphere at about 900°C to diffuse the aforementioned n-type impurity (P) and p-type impurity, as shown in Fig. 7, there are formed the n-type semiconductor regions 11 (the source regions and the drain regions) of the memory cell selecting MISFETs, an n^--type semiconductor region 12 and an

n^+-type semiconductor region 13 of the n-channel MISFETs of the peripheral circuit, and a p^--type semiconductor region 14 and a p^+-type semiconductor region 15 of the p-channel MISFETs. The n^+-type semiconductor region 13 and the p^+-type semiconductor region 15 are formed in self-alignment with the side wall spacers 10. In the peripheral circuit, the source regions and the drain regions of the n-channel MISFETs are individually constructed of an LDD (Lightly Doped Drain) structure composed of the n^--type semiconductor region 12 and the n^+-type semiconductor region 13, and the source regions and the drain regions of the p-channel MISFETs are individually constructed of an LDD structure composed of the p^--type semiconductor region 14 and the p^+-type semiconductor region 15.

Next, as shown in Fig. 8, contact holes 17 and 18 for exposing a portion of the semiconductor region 11 to the outside are formed over the n-type semiconductor regions 11 (the source regions and the drain regions) of the n-type semiconductor regions 11 of the memory cell selecting MISFETs; contact holes 19 and 20 for exposing portions of the semiconductor regions 12 and 13 to the outside are formed over the n^+-type semiconductor regions 13 (the source regions

and the drain regions) of the n-channel MISFETs of the peripheral circuit; and contact holes 21 and 22 for exposing portions of the semiconductor regions 14 and 15 to the outside are formed over the p^+-type semiconductor regions 15 (the source regions and the drain regions) of the p^+-type semiconductor regions 15 of the p-channel MISFETs, by depositing a silicon oxide film 16 having a thickness of about 500 nm at a filming temperature of about 390°C over the memory cell selecting MISFETs, the n-channel MISFETs and the p-channel MISFETs of the peripheral circuit by a plasma CVD method, by polishing the silicon oxide film 16 by a CMP (Chemical-Mechanical Polishing) method to flatten its surface, and by etching the silicon oxide film 15 and the gate oxide film 7 by using a photoresist as the mask.

At this time, the silicon nitride film 9, formed over the gate electrodes 8A (the word lines WL) of the memory cell selecting MISFETs, and the side wall spacers 10 of silicon nitride, formed at the side walls, are slightly etched so that the contact holes 17 and 18 are formed in self-alignment with the side wall spacers. Likewise, the silicon nitride film 9, formed over the gate electrodes 8B of the n-channel MISFETs of the peripheral circuit and over the gate

electrodes 8C of the p-channel MISFETs, and the side wall spacers 10 of silicon nitride, formed at the side walls, are slightly etched, so that the contact holes 19 to 22 are formed in self-alignment with the side wall spacers 10.

The insulating film to be formed over the memory cell selecting MISFETs and the n-channel MISFETs and p-channel MISFETs of the peripheral circuit should not be limited to the aforementioned silicon oxide film 16 but can be an ozone (O_3)-BPSG (Boron-doped Phospho Silicate Glass) film deposited at a filming temperature of about 450°C by a CVD method, or an ozone-TEOS (Tatra Ethoxy Silane) film deposited at a filming temperature of about 400°C by a CVD method. These insulating films are flattened at their surfaces by the chemical-mechanical polishing (CMP) method, as for the silicon oxide film 16.

Next, as shown in Fig. 9, plugs 23, made of a multilayer film of titanium nitride (TiN) and W, are buried in the contact holes 17 to 22. These plugs 23 are formed by depositing a TiN film having a thickness of about 50 nm acting as an adhesive layer for the substrate and the W film over the silicon oxide film 16 by a sputtering method, by depositing the W film having a thickness of about 300 nm at a filming

temperature of 475°C over the TiN film by a CVD method, and by etching back the W film and the TiN film.

At this time, in order to reduce the contact resistance between the plugs 23 and the substrate, a Ti silicide ($TiSi_2$) film may be formed below the contact holes 17 to 22. This Ti silicide film is formed by depositing a Ti film having a thickness of about 50 nm over the silicon oxide film 16 by a sputtering method, by causing the Ti film and the semiconductor substrate below the contact holes 17 to 22 to react by annealing them at a temperature of about 800°C, and by wet-etching off the Ti film left unreacted over the silicon oxide film 16. After this, the TiN film and W film, deposited over the silicon oxide film 16, are etched back to form the plugs 23.

Next, as shown in Fig, 10, bit lines BL_1 and BL_2 and wiring lines 24A and 24B of the peripheral circuit are formed over the silicon oxide film 16. These bit lines BL_1 and BL_2 and the wiring lines 24A and 24B are simultaneously formed by depositing a W film having a thickness of about 300 nm at a filming temperature of about 475°C over the silicon oxide film 16 by a plasma CVD method, by depositing a silicon nitride film 25 having a thickness of about 200 nm at a filming

temperature of about 360°C over that W film by a plasma CVD method, and by etching and patterning those films by using a photoresist as the mask.

The bit line BL_1 is electrically connected through the aforementioned contact hole 17 with one of the source region and the drain region (the n-type semiconductor regions 11) of the memory cell selecting MISFET. The bit line BL_2 is extended from the memory array region to the peripheral circuit region and is electrically connected through the aforementioned contact hole 19 with one of the source region and the drain region (the n^+-type semiconductor regions 13) of an n-channel MISFET Qn of the peripheral circuit.

One end of the wiring line 24A of the peripheral circuit is electrically connected through the contact hole 20 with the other (the n^+-type semiconductor region 13) of the source region and the drain region of the n-channel MISFET, and the other end of the wiring line 24A is electrically connected through the contact hole 21 with one of the source region and the drain region (the p^+-type semiconductor regions 15) of the p-channel MISFET. The wiring line 24B is electrically connected through the contact hole 22 with the other (the p^+-type semiconductor region 15) of the source region and the drain region of the

p-channel MISFET.

Next, as shown in Fig. 11, side wall spacers 26 are formed at the individual side walls of the bit lines BL_1 and BL_2 and the wiring lines 24A and 24B. These side wall spacers 28 are formed by depositing a silicon nitride film having a thickness of about 100 nm at a filming temperature of about 360°C over the silicon oxide film 16 by a plasma CVD method, and by working the silicon nitride film by an anisotropic etching method.

Next, as shown in Fig. 12, contact holes 28 for exposing the plugs 23 in the contact holes 18 to the outside are formed over the contact holes 18, formed to expose the upper portion of one of the n-type semiconductor regions 11 (the source region and the drain region) of the memory cell selecting MISFET, by depositing a silicon oxide film 27 having a thickness of about 500 nm at a filming temperature of about 390°C over the bit lines BL_1 and BL_2 and the wiring lines 24A and 24B by a plasma CVD method, by polishing the silicon oxide film 27 by a chemical mechanical polishing (CMP) method to flatten its surface, and by etching the silicon oxide film 27 by using a photoresist as the mask. At this time, the silicon oxide film 25, formed over the bit line BL_1, and the

side wall spacers 26 of silicon nitride, formed at the side walls, are slightly etched so that the contact holes 28 are formed in self-alignment with the side wall spacers 26.

The insulating film to be deposited over the bit lines BL_1 and BL_2 and the wiring lines 24A and 24B should not be limited to the aforementioned silicon oxide film 27 but can be the aforementioned ozone-BPSG film or ozone-TEOS film, or an SOG (Spin On Glass) film. The ozone-BPSG film or ozone-TEOS film is flattened, if employed, on its surface by a chemical mechanical polishing (CMP) method as for the silicon oxide film 27.

Next, as shown in Fig. 13, W plugs 30 are buried in the contact holes 28, and storage electrodes (lower electrodes) 32 of information storing capacitive elements are formed over the contact holes 28. The W plugs 30 are formed by depositing a W film having a thickness of about 300 nm at a filming temperature of about 500°C over the silicon oxide film 27 by a CVD method, and by etching back the W film. The storage electrodes 32 are formed by depositing a W film having a thickness of about 500 nm at a filming temperature of about 475°C over the silicon oxide film 27 by a CVD method, and by pattering the W film by using a

photoresist as the mask. The W film constituting the plugs 30 is deposited at a higher filming temperature (500°C) than that (475°C) of the W film constituting the storage electrodes 32, because it is required to retain the coverage of the inside of the contact holes 28.

Next, as shown in Fig. 14, there are formed over the storage electrodes 32, a capacitor insulating film 33 and plate electrodes (upper electrodes) 34 of the information storing capacitive elements. The capacitor insulating film 33 and the plate electrodes 34 are simultaneously formed by depositing a Ta_2O_5 film having a thickness of about 15 nm at a filming temperature of about 400 to 480°C over the storage electrodes 32 by a CVD method, by depositing a TiN film having a thickness of about 150 nm over the Ta_2O_5 film by a sputtering method, and by etching and patterning those films by using a photoresist as the mask. As a result, there is formed an information storing capacitive element C of the memory cell, which is composed of the storage electrode 32, the capacitor insulating film 33 and the plate electrode 34.

Next, as shown in Fig. 15, a contact hole 36 is formed over the plate electrode 34 of the information storing capacitive element C by depositing a silicon

oxide film 35 having a thickness of about 500 nm at a filming temperature of about 390°C over the information depositing capacitive element C by a plasma CVD method, and by etching the silicon oxide film 35 by using a photoresist as the mask. Simultaneously with this, a contact hole 37 is formed over the wiring line 24A of the peripheral circuit, and a contact hole 38 is formed over the wiring line 24B, by etching the silicon oxide film 35, the silicon oxide film 27 and the silicon nitride film 25. The insulating film to be deposited over the information storing capacitive element C should not be limited to the aforementioned silicon oxide film 35 but can be a three-layered insulating film in which a spin-on-glass film is sandwiched between the two silicon oxide films 35.

Next, as shown in Fig. 16, wiring lines 39A, 39B, 39C and 39D are formed over the silicon oxide film 35. These wiring lines 39A, 39B, 39C and 39D are simultaneously formed by depositing a TiN film having a thickness of about 50 nm, an Aℓ (aluminum) alloy film having a thickness of about 500 nm and a TiN film having a thickness of about 10 nm over the silicon oxide film 35 at a substrate temperature of 300 to 350°C by a sputtering method, and etching and

patterning those films by using a photoresist as the mask. By the steps thus far described, the DRAM of the present embodiment is substantially completed.

By the DRAM manufacturing process of the present embodiment, at the step after the individual source regions and drain regions of the memory cell selecting MISFET and the n-channel MISFET and the p-channel MISFET of the peripheral circuit have been formed, the wiring conductive film and the insulating film are deposited at a temperature of 500°C or lower, so that the diffusion of the impurity into the substrate by the high-temperature heat treatment can be suppressed to realize a shallow junction between the source regions and the drain rations thereby to enhance the high performance of the DRAM.

By the DRAM manufacturing process of the present embodiment, all the wiring conductive films are made of metal materials (W or Aℓ) or the metal compound material (TiN) so that the wiring resistance which may rise because of the miniaturization, can be lowered to increase the speedup of the DRAM. The wiring conductive film should not be limited to the material employed in the present embodiment but can be made of Ti or copper (Cu), for example.

(Embodiment 2)

In the foregoing Embodiment 1, the gate electrodes 8A of the memory cell selecting MISFET and the gate electrodes 8B of the n-channel MISFET and the gate electrodes 8C of the p-channel MISFET of the peripheral circuit are individually composed of the tungsten (W) film which is deposited at the filming temperature of about 475°C. In the present embodiment, however, the gate electrodes 8A (the word lines WL) and the gate electrodes 8B and 8C are composed of a multilayer film of a polycrystalline silicon film, a titanium nitride (TiN) film and a tungsten (W) film, as shown in Fig. 17.

In this case, the polycrystalline silicon film having a thickness of about 250 nm is deposited at first at a filming temperature of about 540°C by a CVD method, and the titanium nitride (TiN) having a thickness of about 50 nm for an adhesive layer between the polycrystalline silicon film and the tungsten (W) film is then deposited over the polycrystalline silicon film by a sputtering method. The polycrystalline silicon film is doped with an n-type impurity or phosphor (P) of about 1.5×10^{20} cm^{-3}. The titanium nitride prevents the polycrystalline silicon film and the tungsten (W) film from reacting to form a tungsten silicide (WSi) film. This is because the

resistance rises if the tungsten turns into the tungsten silicide.

Next, the gate electrodes 8A (the word lines WL) and the gate electrodes 8B and 8C are simultaneously formed by depositing a W film having a thickness of about 100 nm at a filming temperature of about 475°C over the TiN film by a CVD method, by depositing the silicon nitride film 9 having a thickness of about 250 nm at a filming temperature of about 360°C over the W film by a plasma CVD method, and by etching and patterning the silicon nitride film 9, the W film, the TiN film and the polycrystalline silicon film by using a photoresist as the mask. The other steps are identical to those of foregoing Embodiment 1, and a DRAM is completed by applying the steps after the step of forming the gate electrodes 8A, 8B and 8C.

By the DRAM manufacturing process of the present embodiment, the wiring conductive film and the insulating film are deposited at a temperature of 500°C or lower after the individual source regions and drain regions of the memory cell selecting MISFET and the n-channel MISFET and the p-channel MISFET of the peripheral circuit have been formed, so that the high performance of the DRAM can be enhanced.

By the DRAM manufacturing process of the present

embodiment, the high speed of the DRAM can be increased as in Embodiment 1 by making all the wiring conductive films of a material containing a metal material or a metal compound.

(Embodiment 3)

In order to manufacture a DRAM of the present embodiment, as shown in Fig. 18, the surface of the semiconductor substrate 1 of p^--type single crystal silicon is thermally oxidized at first to form a thin silicon oxide film 43, and a silicon nitride film 44 is then deposited over the silicon oxide film 43 by a CVD method. The silicon nitride film 44 is etched by using a photoresist as the mask, and it is removed from the element isolating region.

Next, as shown in Fig. 19, the semiconductor substrate 1 at the element isolating region is etched by using the silicon nitride film 44 as the mask to form shallow grooves 52 having a depth of about 0.35 μm, and a silicon oxide film 53 having a thickness of about 10 nm is then formed in the shallow groove 52.

Next, as shown in Fig. 20, a silicon oxide film 54 is buried in the shallow groove 52. In order to bury the silicon oxide film 54 in the shallow groove 52, the silicon oxide film 54 having a thickness of about 600 nm is deposited over the semiconductor

substrate 1 by a CVD method and is then polished by a chemical-mechanical polishing (CMP) method. After this, the silicon nitride film 44, left over the semiconductor substrate 1, is etched off.

Next, as shown in Fig. 21, a p-type well 3 is formed by doping the semiconductor substrate 1 with ions of a p-type impurity or boron (B) by using the (not-shown) photoresist for exposing the region for forming the memory array and the region for forming the n-channel MISFET of the peripheral circuit selectively to the outside, and the n-type well 4 is formed by doping the semiconductor substrate 1 with ions of an n-type impurity or phosphor (P) by using the (not-shown) photoresist exposing the region for forming the p-channel MISFET of the peripheral circuit selectively to the outside. For this doping, the peaks of the individual distributions of the n-type impurity and the p-type impurity are substantially equalized to the depth of the shallow groove 52, so that the p-type or n-type semiconductor regions are formed in the semiconductor substrate at the bottom of the shallow groove 52. As a result, the p-type well 3 acts as a p-type channel stopper layer, and the n-type well 4 acts as an n-type channel stopper layer.

Next, as shown in Fig. 22, the surfaces of the

individual active regions of the p-type well 3 and the n-type well 4, enclosed by the shallow groove 52, are thermally oxidized at a temperature of about 800°C to form the gate oxide film 7 having a thickness of about 8 nm. The subsequent steps are identical to those of Embodiment 1.

By the DRAM manufacturing process of the present embodiment, the p-type well 3 acts as the p-type channel stopper layer whereas the n-type well 4 acts as the n-type channel stopper layer. As a result, the ion implantation for forming the p-type channel stopper layer and the ion implantation for forming the n-type channel stopper layer can be eliminated to simplify the DRAM manufacturing process more than the process of Embodiment 1.

By the DRAM manufacturing process of the present embodiment, the elements are isolated by the shallow groove 52, formed in the semiconductor substrate 1, so that the miniaturization of the DRAM can be promoted. Since the step between the element isolating region and the active region is eliminated, moreover, it is possible to prevent the drawback that the conductive film such as the gate electrode material, deposited over the semiconductor substrate 1, is thinned at the step portion.

Moreover, the step between the element isolating region and the active region can be made less than the LOCOS of the prior art so that microminiaturization process can be performed at the step of patterning the conductive film such as the gate electrode material deposited over the semiconductor substrate.

The present embodiment can be combined with other Embodiments of the present invention,

(Embodiment 4)

In order to manufacture the DRAM of the present embodiment, by the manufacture process of Embodiment 1, the contact holes 17 and 18 for exposing a portion of the semiconductor region 11 are formed by forming the memory cell selecting MISFET, and the n-channel MISFET and the p-channel MISFET of the peripheral circuit, by depositing the silicon oxide film 16 over those MISFETs, by polishing the silicon oxide film 16 by a chemical mechanical-polishing (CMP) method to flatten its surface, and by etching the silicon oxide film 16 and the gate oxide film 7 by using a photo-resist as the mask to form the contact holes 17 and 18 over the n-type semiconductor region 11 (the source region and the drain region) of the memory cell selecting MISFET.

This not-shown photoresist mask is patterned to

cover the peripheral circuit forming region and to have openings over the n-type semiconductor region 11 or the source and drain of the memory cell selecting MISFET.

Next, as shown in Fig. 24, the plugs 29 of polycrystalline silicon are buried in the contact holes. These plugs 29 are formed by depositing the polycrystalline silicon film having a thickness of about 360 nm at a filming temperature of about 540°C over the silicon oxide film 16 by a CVD method, and by etching back the polycrystalline silicon film (while leaving the polycrystalline silicon film only in the contact holes 17 and 18). This polycrystalline silicon film is doped with an n-type impurity of phosphor (P).

Next, as shown in Fig, 25, a titanium (Ti) silicide layer 31 is formed on the surfaces of plugs 29 of polycrystalline silicon. The titanium silicide layer 31 is formed by burying the polycrystalline silicon plugs 29 in the contact holes 17 and 18, by depositing, just after the burying step, a Ti film having a thickness of about 50 nm over the silicon oxide film 16 by a sputtering method, by annealing the Ti film and the polycrystalline silicon (the plugs 29) at a temperature of about 800°C to react, and by

removing the Ti film, left unreacted over the silicon oxide film 16, by a wet etching.

Next, as shown in Fig. 26, the contact holes 19 and 20 are formed over the n^+-type semiconductor region 13 (the source region and the drain region) of the n-channel MISFET of the peripheral circuit, and the contact holes 21 and 22 are formed over the p^+-type semiconductor region 15 (the source region and the drain region) of the p-channel MISFET, by depositing a silicon oxide film 45 having a thickness of about 50 nm at a filming temperature of about 360°C over the silicon oxide film 16 by a plasma CVD method, and by etching the silicon oxide film 45, the silicon oxide film 16 and the gate oxide film 7 by using as the mask a photoresist covering the memory cells and having openings over the semiconductor regions 13 of the n-channel MISFET and the semiconductor regions 15 of the p-channel MISFET of the peripheral circuit region.

Next, as shown in Fig. 27, the plugs 23, composed of the multilayer film of TiN and W, are buried in the contact holes 19 to 22 of the peripheral circuit in accordance with the process of Embodiment 1. After this, the silicon oxide film 45 of the contact holes 17, formed over one (located at the side for connecting the bit lines) of the n-type semiconductor

regions 11 (the source region and the drain region) of the memory cell selecting MISFET, is removed to expose the surface of the titanium silicide layer 31, formed over the surfaces of the plugs 29, to the outside. After this, as shown in Fig. 28, the bit lines BL_1 and BL_2 and the wiring lines 24A and 24B of the peripheral circuit are formed over the silicon oxide film 45, and the side wall spacers 26 are then formed at the individual side walls of the bit lines BL_1 and BL_2 and the wiring lines 24A and 24B. The methods for forming the insulating film 25 over the bit lines BL_1 and BL_2 and the side wall spacers 26 are similar to those of Embodiment 1.

Next, as shown in Fig. 29, by the process of Embodiment 1, the contact holes 28 are formed in self-alignment with the side wall spacers 26 of the side walls of the bit lines BL_1 and BL_2 over the aforementioned contact holes 18, formed over one of the n-type semiconductor regions 11 (the source region and the drain region) of the memory cell selecting MISFET, by depositing the silicon oxide film 27 individually over the bit lines BL_1 and BL_2 and the wiring lines 24A and 24B, by polishing and flattening the surface of the silicon oxide film 27 by a chemical-mechanical polishing (CMP) method, and by

etching the silicon oxide film 27 by using a photo-resist as the mask.

Next, as shown in Fig. 30, foreign matters on the surface of the aforementioned Ti silicide layer 30, exposed at the bottoms of the contact holes 28, is removed by a sputter-etching method using argon (Ar), and the plugs 30 of polycrystalline silicon or W are buried in the contact holes 28. If, at this time, the Ti silicide film 31 is not formed on the surfaces of the polycrystalline silicon plugs 29, the contact resistance is increased between the surfaces of the plugs 29 (of polycrystalline silicon) are oxidized at the time of burying the plugs 30 in the contact holes 28. If, at this time, the wet etching is executed to remove the oxide film from the surfaces of the plugs 29 (of polycrystalline silicon), the insulating film 27 in the bottoms and at the sides of the contact holes 28 are side-etched to cause the shape defect of the contact holes 28. For the plugs 29 made of polycrystalline silicon, the oxide film to be formed over the surfaces cannot be removed by a dry etching method, but a wet etching method is essential.

By the DRAM manufacturing process of the present embodiment, the Ti silicide layer 31 is formed on the surfaces of the aforementioned polycrystalline silicon

plugs 29, buried in the contact holes 18, is formed to reduce the oxidation of the surfaces of the plugs 29 (polycrystalline silicon) so that the oxide film can be removed not by an isotropic wet etching method but only by a dry etching method using Ar. As a result, there arises none of the aforementioned problems. In short, the contact resistance can be reduced without causing the shape defect of the contact holes 28.

In order to prevent the oxidation of the surfaces of the plugs 29 (polycrystalline silicon), a metal film of Ti or the like may be selectively grown on the surfaces of the polycrystalline silicon plugs 29 immediately after the plugs 29 have been buried in the contact holes 17 and 18.

Next, as shown in Fig. 31, by the process of Embodiment 1, the contact holes 36 are formed over the plate electrodes 34 of the information storing capacitive element C after forming the information storing capacitive element C over the contact holes 28, by depositing the silicon oxide film 35 over the information storing capacitive element C, and by etching the silicon oxide film 35 by using a photoresist as the mask. Simultaneously with this, by etching the silicon oxide film 35 and the silicon oxide film 27, the contact holes 37 are formed over

the wiring lines 24A of the peripheral circuit, and the contact holes 38 are formed over the wiring lines 24B.

Next, as shown in Fig. 32, plugs 55 of TiN are buried in the contact holes 35, 36 and 37. These TiN plugs 55 are formed by depositing the TiN film over the silicon oxide film 35 by using a sputtering method and a CVD method, and by etching back the TiN film.

If the plugs 55 are composed of a multilayer film of TiN and W, the TiN film and the W film are deposited over the silicon oxide film 35 and are then etched back. In this case, the TiN and the W have different etching rates so that the surface of the W film, buried in the contact holes 36, 37 and 38, is excessively etched off if the TiN film over the silicon oxide film 35 is completely removed. This may cause breakage of Aℓ wiring lines over the contact holes 36, 37 and 38 if the Aℓ wiring lines are formed over the silicon oxide film 35. If the TiN film is not completely etched off but left over the silicon oxide film 35, on the other hand, separation may occur at the interface between the TiN film and the Aℓ wiring lines when these wiring lines are formed thereover.

By the DRAM manufacturing process of the present

embodiment, the aforementioned drawbacks can be avoided by making the plug material to be buried in the contact holes 36, 37 and 38, of a single layer of TiN.

Next, as shown in Fig. 33, the wiring lines 39A, 39B, 39C and 39D are formed over the silicon oxide film 35. Specifically, these wiring lines 39A, 39B, 39C and 39D are formed by depositing an Aℓ alloy film having a thickness of about 500 nm and a TiN film having a thickness of about 10 nm over the silicon oxide film 35 by a sputtering method, and by etching and patterning those films by using a photoresist as the mask. After the steps thus far described, the DRAM of the present embodiment is substantially completed. It is needless to say that Embodiments 2 and 3 can be applied to the present embodiment.

(Embodiment 5)

In the DRAM of the present embodiment, the conductive material (TiN) constituting the plate electrodes 34 of the information storing capacitive element C is used as the material for the wiring lines of the peripheral circuit, and the plate electrodes 34 and the wiring lines of the peripheral circuits are formed at the common step.

For manufacturing this DRAM by the manufacture

process of Embodiment 1, the capacitor insulating film 33 and the plate electrodes 34 of the information storing capacitive element C are formed simultaneously with wiring lines 56 and 57 of the peripheral circuit, by forming the storage electrodes 32 of the information storing capacitive element over the silicon oxide film 27, deposited over the bit lines BL_1 and BL_2 and the wiring lines 24A and 24B of the peripheral circuit, as shown in Fig. 34, and by patterning the Ta_2O_5 film and the TiN film deposited over the storage electrodes 32, as shown in Fig. 35.

The wiring lines 56 and 57, formed of the multilayer film of the Ta_2O_5 film or the capacitor insulating film and the TiN film deposited over the former, cannot be connected directly with the underlying wiring lines through the contact holes. In this case, if the TiN film is deposited after the Ta_2O_5 has been deposited and then etched off from the peripheral circuit, the direct connection with the underlying wiring lines can be made but increases the number of steps. Since the Ta_2O_3 is partially etched off, moreover, the reliability of the capacitor insulating film may drop. Specifically, a photoresist film of a predetermined pattern is formed over the capacitor insulating film 33, and this capacitor

insulating film 33 is etched. After this, the quality of the capacitor insulating film 33 is deteriorated by the ashing treatment with O_2 for removing the photoresist. In the present embodiment, therefore, the wiring lines 58 and 57 and the underlying wiring lines are connected by the following method.

First of all, as shown in Fig. 36, the contact holes 36 are formed over the plate electrodes 34 of the information storing capacitive element C by depositing the silicon oxide film 35 over the information storing capacitive element C and the wiring lines 56 and 57, and by etching the silicon oxide film 35 by using a photoresist as the mask. Simultaneously with this, the contact holes 37 are formed over the wiring lines 24A of the peripheral circuit, and the contact holes 38 are formed over the wiring lines 24B, by etching the silicon oxide film 35, the silicon oxide film 27 and the silicon nitride film 25 in the regions having the wiring lines 56 and 57. At this time, one end of the wiring line 56 is exposed to the inside of the contact hole 37, and one end of the wiring line 57 is exposed to the inside of the contact hole 38.

Next, as shown in Fig. 37, the TiN plugs 55 are buried in the contact holes 36, 37 and 38, and the

wiring lines 39A, 39B, 39C and 39D are then formed over the silicon oxide film 35. As a result, the wiring line 56 is connected through the wiring line 39C with the underlying wiring line 24A, and the wiring line 57 is connected through the wiring line 39D with the underlying wiring line 24B.

By the DRAM manufacturing process of the present embodiment, by using a common material for the plate electrode (TiN) of the information storing capacitive element C and the wiring of the peripheral circuit, the wiring layers of the peripheral circuit can be increased to improve the degree of freedom of the wiring design.

By the DRAM manufacturing process of the present embodiment, the wiring layers of the peripheral circuit can be increased without any increase in the number of steps of manufacturing the DRAM.

(Embodiment 6)

In the DRAM manufacturing process of Embodiment 5, the contact hole 37 is formed over the wiring line 24A by etching the silicon oxide film 35, the silicon oxide film 27 and the silicon nitride film 25 in the regions having the wiring lines 56 and 57 of the peripheral circuit, and the contact hole 38 is formed over the wiring line 24B, so that one end of the

wiring line 56 is exposed to the inside of the contact hole 37 whereas one end of the wiring line 57 is exposed to the inside of the contact hole 38 (as shown in Fig, 36). If, at this time, the etching selection rate of the wiring material (TiN) to the insulating films (the silicon oxide film and the silicon nitride film) is small, the plate electrode 34 and the wiring lines 56 and 57 may be etched to reduce the film thickness. In the present embodiment, therefore, the wiring lines 56 and 57 and the underlying wiring lines are connected by the following method.

First of all, as shown in Fig. 38, the capacitor insulating film 33 and the plate electrode 34 of the information storing capacitive element C are formed simultaneously with the wiring lines 56 and 57 of the peripheral circuit by patterning the Ta_2O_5 film, the TiN film and a third film (a high selection ratio film 58), deposited over the storage electrodes 32. The high selection ratio film 58 may be either the insulating film or the conductive film if it is made of a material having a high etching selection ratio to the silicon oxide film or the silicon nitride film. A suitable film may be a tungsten (W) film.

Next, as shown in Fig. 39, the contact holes 36 are formed over the plate electrode 34 of the

information storing capacitive element C by etching the silicon oxide film 35, deposited over the information storing capacitive element C and the wiring lines 56 and 57, by using a photoresist as the mask. Simultaneously with this, the contact hole 37 is formed over the wiring line 24A of the peripheral circuit, and the contact hole 38 is formed over the wiring line 24B, by etching the silicon oxide film 35, the silicon oxide film 27 and the silicon nitride film 25 in the regions having the wiring lines 56 and 57. Since, at this time, the plate electrode 34 and the wiring lines 56 and 57 are covered with the high selection ratio film 58, the etching of the plate electrode 34 and the wiring lines 56 and 57 does not increase the film thickness.

Next, as shown in Fig. 40, one end of the wiring line 56 is exposed to the inside of the contact hole 37, and one end of the wiring line is exposed to the inside of the contact hole 38 by etching the high selection ratio film 58 covering the plate electrode 34 and the wiring lines 56 and 57, at the final stage of the etching treatment. After this, the wiring lines 39A, 39B, 39C and 39D are formed over the silicon oxide film 35 in accordance with the process of Embodiment 5. Incidentally, this etching step is

unnecessary if the high selection ratio film is made of tungsten.

By the DRAM manufacturing process of the present embodiment, it is possible to reliably prevent the drawback that the plate electrode 34 and the wiring lines 56 and 57 are etched and thinned at the step of forming the contact holes (36, 37 and 38).

The connection between the wiring lines 56 and 57 of the peripheral circuit and the underlying wiring lines may also be effected by the following method.

First of all, as shown in Fig. 41, the capacitor insulating film 33 and the plate electrode 34 are formed simultaneously with the wiring lines 56 and 57 of the peripheral circuit by patterning the Ta_2O_5 film, the TiN film and the high selection ratio film 58, deposited over the storage electrodes 32.

Next, as shown in Fig. 42, the contact hole 37 is formed over the wiring line 24A of the peripheral circuit, and the contact hole 38 is formed over the wiring line 24B, by etching the silicon oxide film 35, the silicon oxide film 27 and the silicon nitride film 25, formed over the wiring lines 56 and 57, by using a photoresist 59 as the mask. At this time, the high selection ratio film 58 covering the wiring lines 56 and 57 acts as the etching stopper to prevent the

wiring lines 56 and 57 from being etched and thinned.

Next, as shown in Fig. 43, one end of the wiring line 56 is exposed inside the contact hole 37, and one end of the wiring line 57 is exposed inside the contact hole 38, by etching the high selection ratio film 58 covering the wiring lines 56 and 57, at the final etching stage,

After this, as shown in Fig. 44, a wiring line 60 is formed over the contact hole 37, and a wiring line 61 is formed over the contact hole 38, by patterning the conductive film, deposited over the silicon oxide film 27. As a result, the wiring line 56 of the peripheral circuit is connected through the wiring line 60 to the underlying wiring line 24A, and the wiring line 57 is connected through the wiring line 61 to the underlying wiring line 24B.

The wiring lines 56 and 57 of the peripheral circuit and the underlying wiring lines may be connected by the following method.

First of all, as shown in Fig. 45, the capacitor insulating film 33 and the plate electrode 34 of the information storing capacitive element C are formed together with the wiring lines 56 and 67 of the peripheral circuit, by patterning the Ta_2O_5 film, the TiN film and the high selection ratio film 58,

deposited over the storage electrodes 32. After this, the contact hole 36 is formed over the plate electrode 34 of the information storing capacitive element C, and the contact hole 37 is formed over the wiring line 56, by etching the silicon oxide film 35, deposited over the information storing capacitive element C and the wiring lines 56 and 57, by using a photoresist as the mask. Simultaneously with this, the contact hole 38 is formed over the wiring line 24B of the peripheral circuit by etching the silicon oxide film 35, the silicon oxide film 27 and the silicon nitride film 25 in the region where the wiring line 57 is formed. At this time, the plate electrode 34 and the wiring lines 56 and 57 are covered with the high selection ratio film 58, so that they are prevented from being etched and thinned.

Next, as shown in Fig. 46, one end of the wiring line 56 is exposed inside of the contact hole 37, and one end of the wiring line 57 is exposed inside the contact hole 38, by etching the high selection ratio film 58 covering the wiring lines 56 and 57, at the final etching state.

Next, as shown in Fig. 47, the TiN plugs 55 are buried in the contact holes 35, 36 and 37, and the wiring lines 39A, 39B and 39C are then formed over the

silicon oxide film 35. As a result, the wiring line 56 of the peripheral circuit is connected through the wiring line 39C and the wiring line 57 with the underlying wiring line 24B.

(Embodiment 7)

The present embodiment is applied to a process for manufacturing a CMOS (Complementary Metal Oxide Semiconductor) FET.

First of all, as shown in Fig. 48, the field oxide film 2 having a thickness of about 400 nm is formed over the surface of the semiconductor substrate 1. The field oxide film 2 is prepared by annealing the semiconductor substrate 1 at a temperature of about 1,000°C by using a silicon nitride film as the mask.

Subsequently, the surface of the semiconductor substrate in the region to form the p-channel MISFET is covered with a photoresist 70, and the semiconductor substrate 1 in the region where the n-channel MISFET is formed is doped with ions of a p-type impurity (B) to form the p-type well 3.

Next, the photoresist 70 is removed, and the semiconductor substrate is annealed to repair the crystal defects which are caused by ion implantation of p-type impurity and is doped all over its surface

with ions of a p-type impurity (B) to form a channel region 72 of the n-channel MISFET. At this time, the semiconductor substrate 1 in the region where the p-channel MISFET is formed is also doped with the ions of p-type impurity.

Next, as shown in Fig. 50, the region where the n-channel MISFET is formed, namely, the p-type well 3 is covered with a photoresist 71, and the semiconductor substrate 1 in the region where the p-channel MISFET is formed is doped twice with the n-type impurity (P) to form the n-type well 4. One of these two ion implantations is to improve the device characteristics and accordingly to introduce the impurity with a relatively low energy. The other ion implantation is to isolate the elements and to reduce the well resistance and accordingly to introduce the impurity with a relatively high energy. The lower-energy ion implantation is the pocket implantation of the PMOS to prevent the short channel effect of the PMOS. On the other hand, the higher-energy ion implantation has a peak impurity concentration at the interface between the field oxide film 2 and the semiconductor substrate 1.

Next, as shown in Fig. 51, the n-type well 4 is doped with ions of an n-type impurity (P) to form a

channel ration 73 of the p-channel MISFET and to compensate the p-type impurity, the ions of which have been introduced at the step of forming the channel region of the aforementioned n-channel MISFET.

Incidentally, in the process described above, after the p-type well 3 has been formed, the photoresist 70 is removed, and the semiconductor substrate is then annealed to repair the crystal defects which has been caused by the ion implantation of the p-type impurity. Despite of this description, however, the p-type well 3 may be doped with ions of p-type impurity while omitting the annealing step to leave the photoresist 70, thereby to form the channel region 72 of the n-channel MISFET.

Moreover, a process, in which the insulating film is buried in the shallow groove of Embodiment 3, can be applied to the element isolating region.

Next, after the photoresist 71 has been removed, the gate oxide film 7 is formed by a thermal oxidizing method over the surfaces of the individual active regions of the p-type well 3 and the n-type well 4, as shown in Fig. 52. Next, the gate electrode 8B of the n-channel MISFET and the gate electrode 8C of the p-channel MISFET are formed over the gate oxide film 7.

The subsequent stops follow the flowchart shown in Fig, 53. Specifically, the impurity activation for forming the source region and the drain region is executed at a temperature of about 900°C. Moreover, the treatment for producing Ti silicide or the like on the bottom of the contact hole so as to lower the contact resistance between the first layer wiring line and the source region or the drain region is executed at 800°C, and the subsequent depositions of the wiring conductive film and the insulating film are executed at 450°C or lower.

The element isolating with the shallow groove is executed according to the flowchart, shown in Fig. 54, as in Embodiment 3. Specifically, the impurity activation for forming the source region and the drain region is executed at a temperature of about 900°C. Moreover, the treatment for forming Ti silicide or the like on the bottom of the contact hole so as to lower the contact resistance between the first layer wiring line and the source region or the drain region is executed at 800°C, and the subsequent depositions of the wiring conductive film and the insulating film are executed at 450°C or lower.

By the CMOSFET manufacturing process of the present embodiment, the formation of the p-type well

and the channel region of the n-channel MISFET and the formation of the n-type well and the channel region of the p-channel MISFET can be made at the totally two photoresist steps thereby to reduce the steps of manufacturing the CMOS LSI.

By the CMOSFET manufacturing process of the present embodiment, the upper limits of the temperatures for the heat treatments are made lower at the later steps so that the diffusion of the impurity into the substrate caused by the hot heat treatment can be suppressed to realize a shallower junction between the source region and the drain region thereby to promote the high performance of the CMOS LSI.

(Embodiment 8)

In the CMOSFET manufacturing process of the present embodiment, as shown in Fig. 55, by the manufacture process of Embodiment 7, the gate electrode 8B of the n-channel MISFET is formed at first over the gate oxide film 7 of the p-type well 3, and the gate electrode 8C of the p-channel MISFET is then formed over the gate oxide film 7 of the n-type well 4.

Next, as shown in Fig. 56, the surface of the n-type well 4 is covered with a photoresist 74, and the p-type well 3 is doped with ions of P and As. At

this time, the ions of P is introduced more deeply and in a less dosage than the ions of As. Alternatively, the ions of P may be obliquely introduced.

Next, after the photoresist 74 has been removed, as shown in Fig. 57, the surface of the p-type well 3 is covered with a photoresist 75, and the n-type well 4 is doped with ions of B.

Next, after the photoresist 75 has been removed, as shown in Fig. 58, an annealing treatment for impurity activation is executed to form the source region and drain region of the n-channel MISFET and the source region and drain region of the p-channel MISFET. The source region and drain region of the n-channel MISFET is constructed of a double diffused drain structure, in which the periphery and bottom portion of an n^+-type semiconductor region 76, heavily doped with diffused As are surrounded by an n^--type semiconductor region 77 lightly doped with diffused P, and the source region and drain region of the p-channel MISFET are constructed of a single diffused drain structure which has a p-type semiconductor region 78.

By the CMOSFET manufacturing process of the present embodiment, the source region and drain region of the n-channel MISFET, constructed of the double

diffused drain, and the source region and drain region of the p-channel MISFET, constructed of the single diffused drain structure, can be formed by totally three ion implantations to simplify the CMOS LSI manufacturing process. Moreover, the source region and drain region of the n-channel MISFET is constructed of the double diffused drain structure so that the high electric field of the end portion of the drain region can be relaxed. As a result, it is possible to suppress the hot electron effect of the n-channel MISFET which raises a problem if the gate length is miniaturized.

Although our invention has been specifically described taking the cases of Embodiments, it should not be limited thereto but can naturally be modified in various manners without departing from the gist thereof.

The effects to be obtained by representatives of the aspect of the invention disclosed herein will be briefly described in the following.

By the manufacture process of the present invention, at the step after the MISFET has been formed, all the conductive films are deposited at a temperature of 500°C or lower over the semiconductor substrate so that the number of heat treatment steps

can be reduced to form a MISFET of shallow junction.

By the manufacture process of the present invention, at the step after the MISFET has been formed, all the insulating films are deposited at a temperature of 500°C or lower over the semiconductor substrate so that the number of heat treatment steps can be reduced to form a MISFET of shallow junction.

By the manufacture process of the present invention, all the conductive films are made of a metal or its compound so that the wiring resistance can be reduced.

By the manufacture process of the present invention, it is possible to simplify the process for manufacturing the semiconductor integrated circuit device having MISFETs.

WE CLAIM:

1. A process for manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a first wiring layer over a main surface of a semiconductor substrate;

(b) forming a first insulating film on the first wiring layer;

(c) forming a second wiring layer which is comprised of first conductor film and a first film formed over the first conductor film over the first insulating film;

(d) forming a second insulating film on the second wiring layer,

(e) the step of forming a first etching mask having openings on the second insulating film,

(f) forming a first contact hole on the second wiring layer in the second insulating film and a second contact hole on the first wiring layer in the first and the second insulating films by etching method through the openings of the first etching mask, wherein the etching ratio of the first film is smaller than the etching ratio of the first and second insulating films by the etching method.

2. A process for manufacturing a semiconductor integrated circuit device according to claim 1, further comprising:

(g) the step of etching the first film exposed in the bottom of the first contact hole.

3. A process for manufacturing a semiconductor integrated circuit device according to claim 1, wherein:

the step (c) further comprising the steps of:

(g) forming the first conductor film over the first insulating film,

(h) forming the first film over the first conductor film,

(i) forming the second etching mask on the first film,

(j) etching the first film and the first conductor film at the area uncovered with the second etching mask.

4. A process for manufacturing a semiconductor integrated circuit device according to claim 1, wherein:

the first film is comprised of second conductor film, wherein the etching ratio of the second conductor film is smaller than the etching ratio of the first conductor film by the etching method.

5. A process for manufacturing a semiconductor circuit device according to claim 4, wherein:

the electric resistance of the first conductor film is smaller than the electric resistance of the second conductor film.

6. A process for manufacturing a semiconductor integrated circuit device according to claim 1, wherein:

tungsten is the main component of the first film.

7. A process for manufacturing a semiconductor integrated circuit device according to claim 1, further comprising the steps of:

(g) forming a electrode over the first insulating film,

(h) forming a dielectric film on the electrode,

before the step (c),

wherein the electrode, dielectric film, and the second wiring layer comprise an information storing capacitive element.

8. A process for manufacturing a semiconductor integrated circuit device according to claim 1, further comprising the steps of:

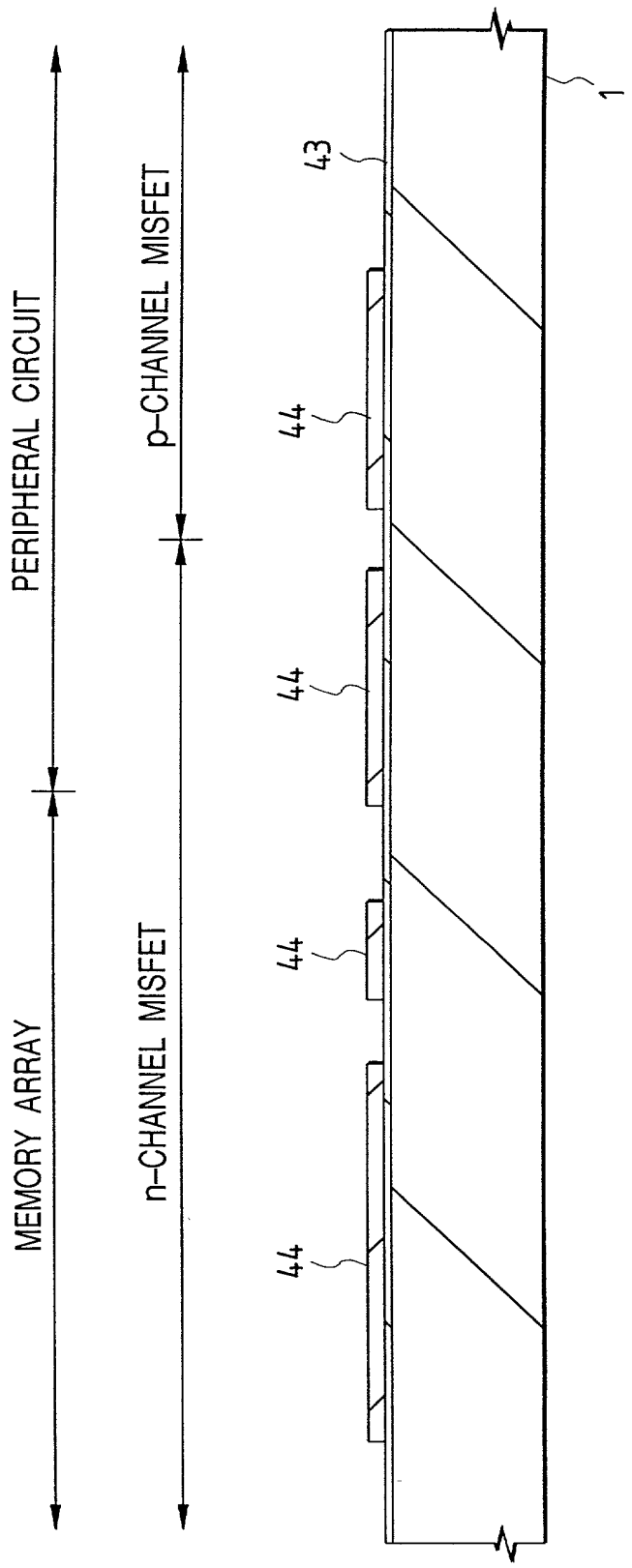
(g) forming second conductor film in the first contact hole and third conductor film in the second contact hole,

(h) forming a third wiring layer electrically connected with the first wiring layer through the second conductor film and a fourth wiring layer electrically connected with the second wiring layer through the third conductor film over the second insulating film.

ABSTRACT OF THE DISCLOSURE

In a process for manufacturing a semiconductor integrated circuit device having a MISFET, in order that a shallow junction between the source/drain of the MISFET and a semiconductor substrate may be realized by reducing the number of heat treatment steps, all conductive films to be deposited on the semiconductor substrate are deposited at a temperature of 500°C or lower at a step after the MISFET has been formed. Moreover, all insulating films to be deposited over the semiconductor substrate are deposited at a temperature of 500°C or lower at a step after the MISFET has been formed.

FIG. 1


PERIPHERAL CIRCUIT
MEMORY ARRAY
p-CHANNEL MISFET
n-CHANNEL MISFET
1
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44
44

FIG. 2

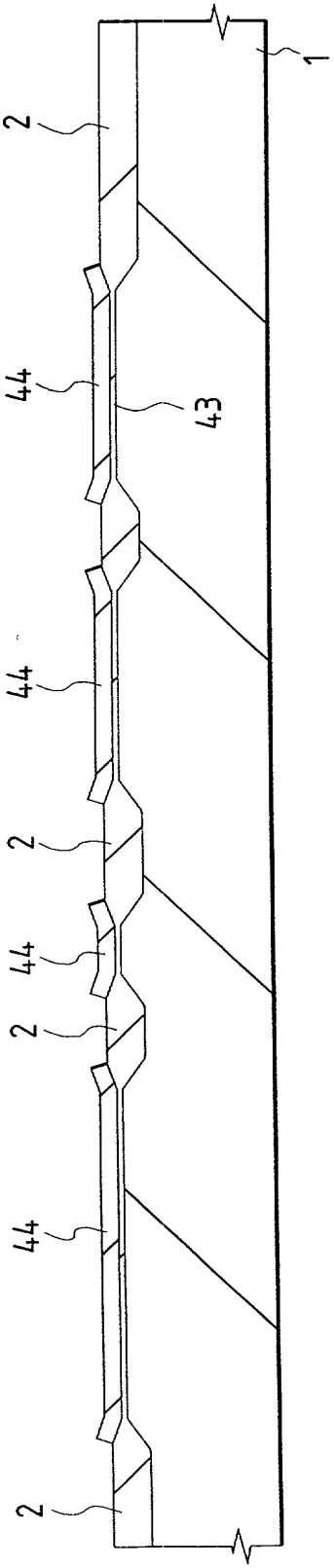

FIG. 3

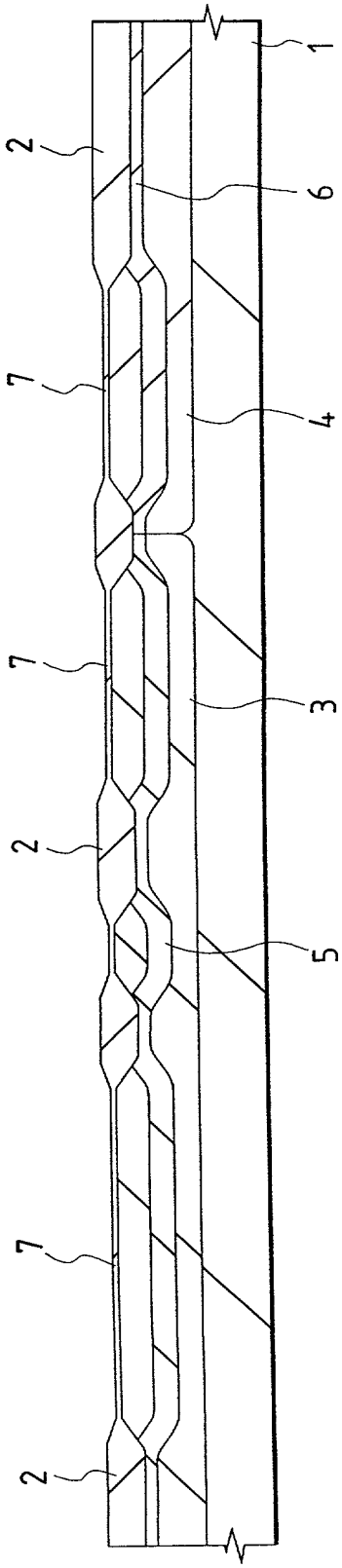

FIG. 4

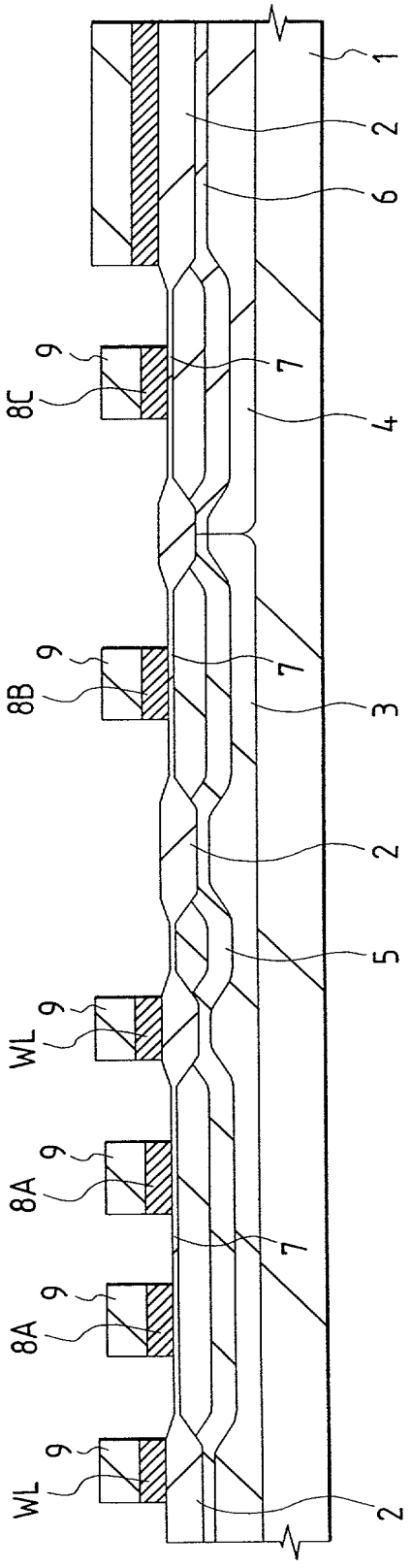

FIG. 5

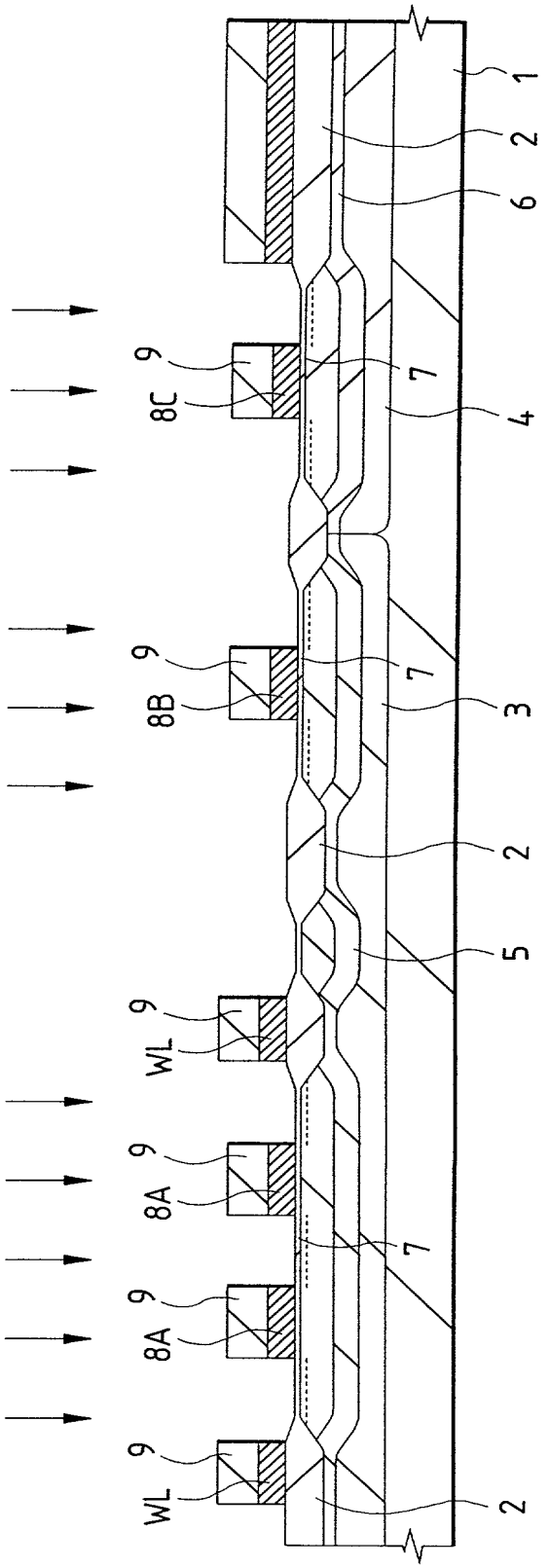

FIG. 6

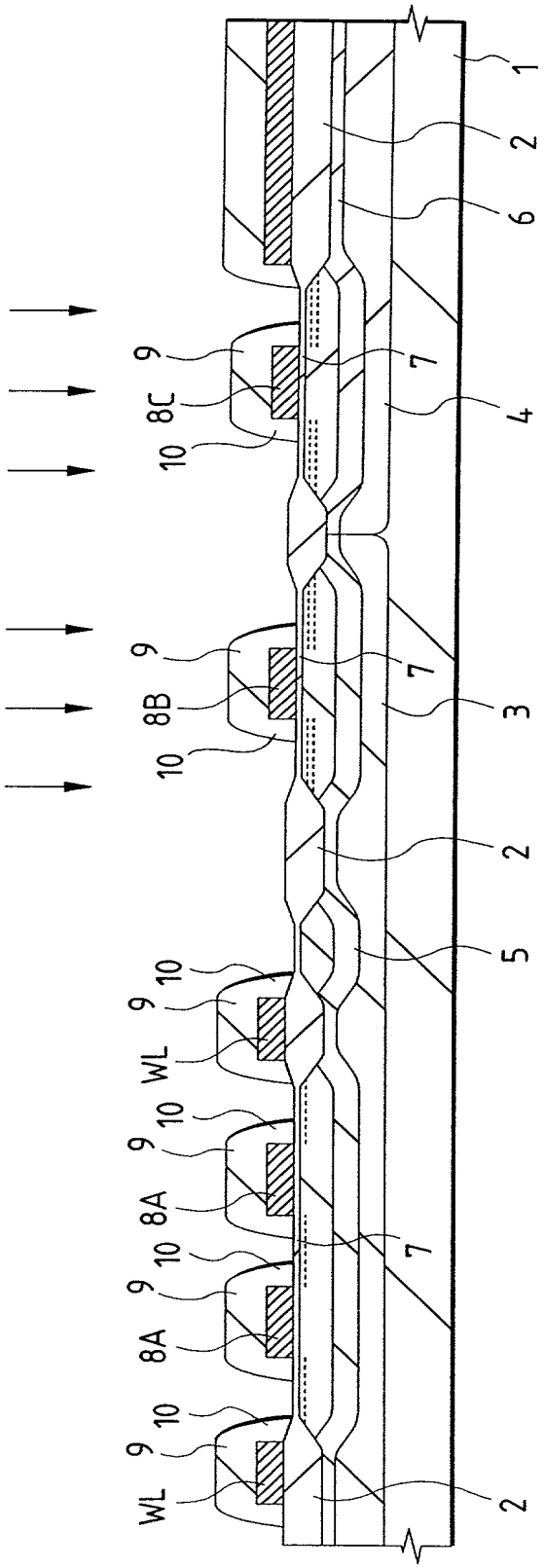

FIG. 7

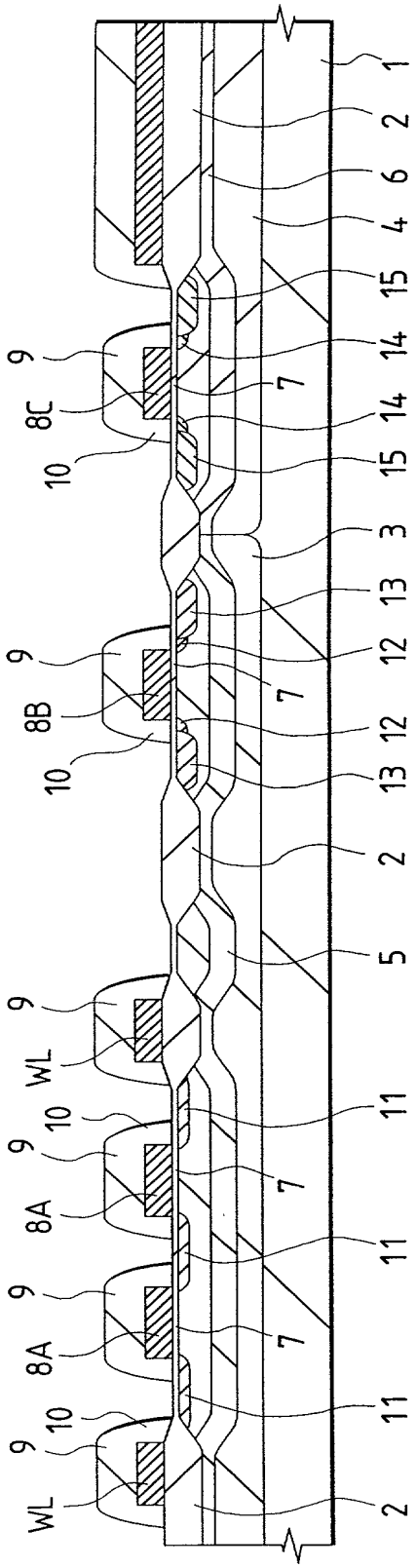
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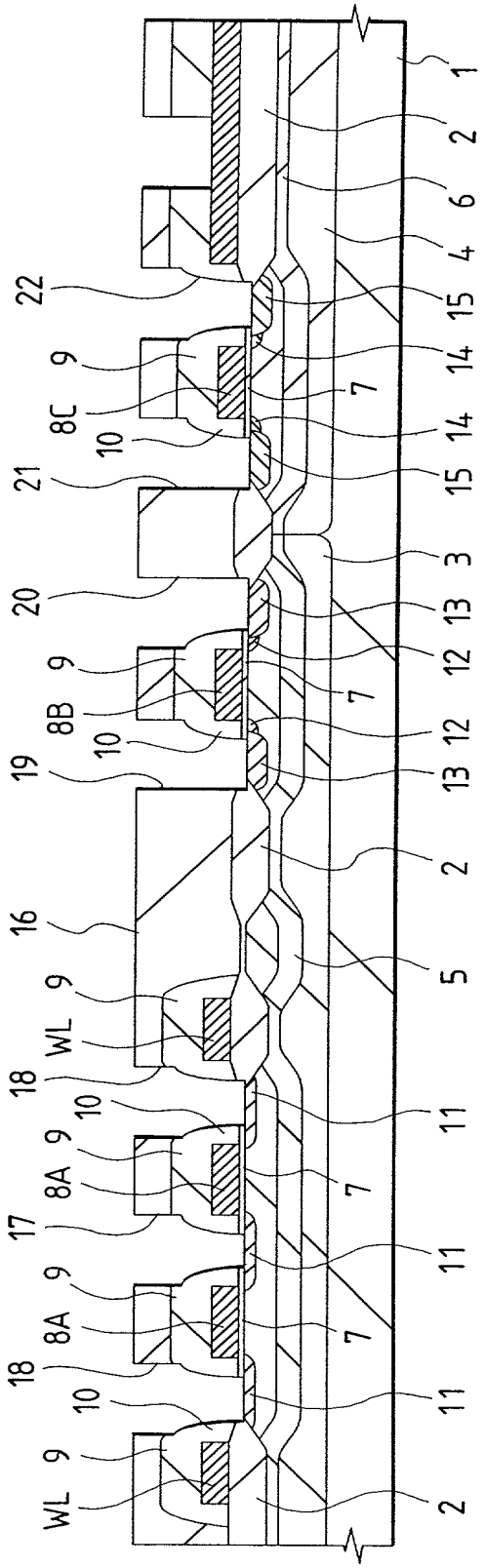
FIG. 8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8C
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WL
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FIG. 9

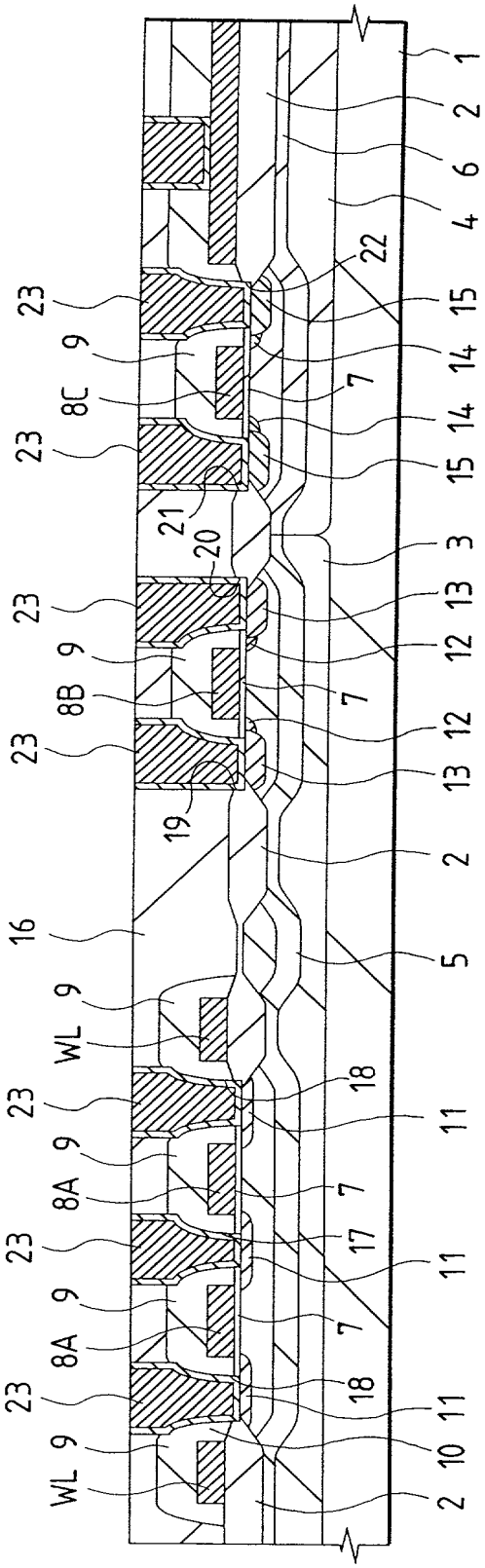
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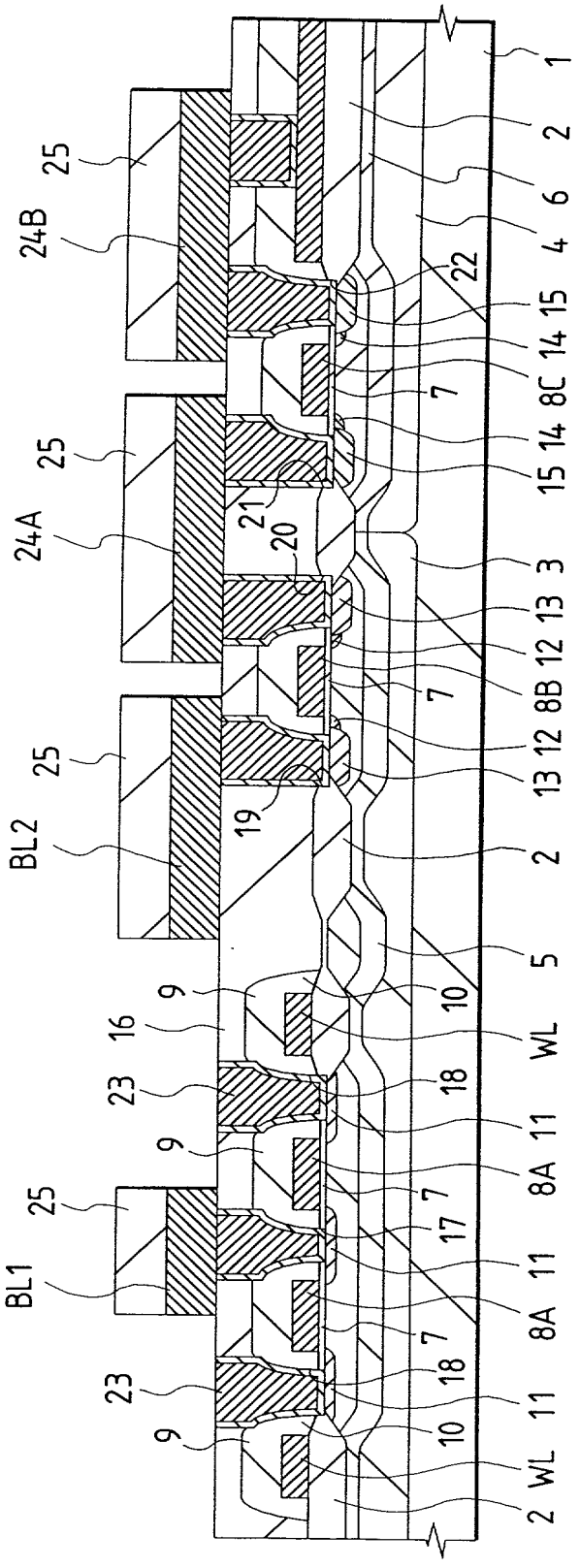
FIG. 10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24B
8A
8B
8C
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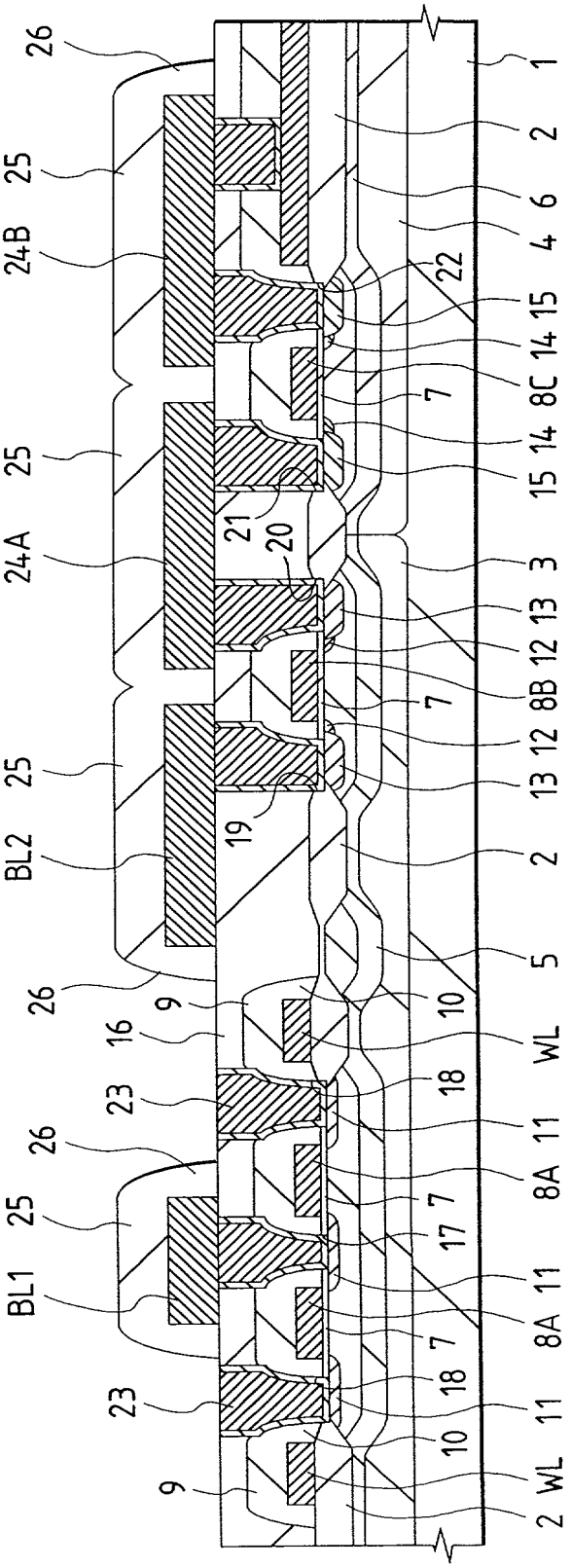
FIG. 11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24B
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24A
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BL2
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26
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BL1
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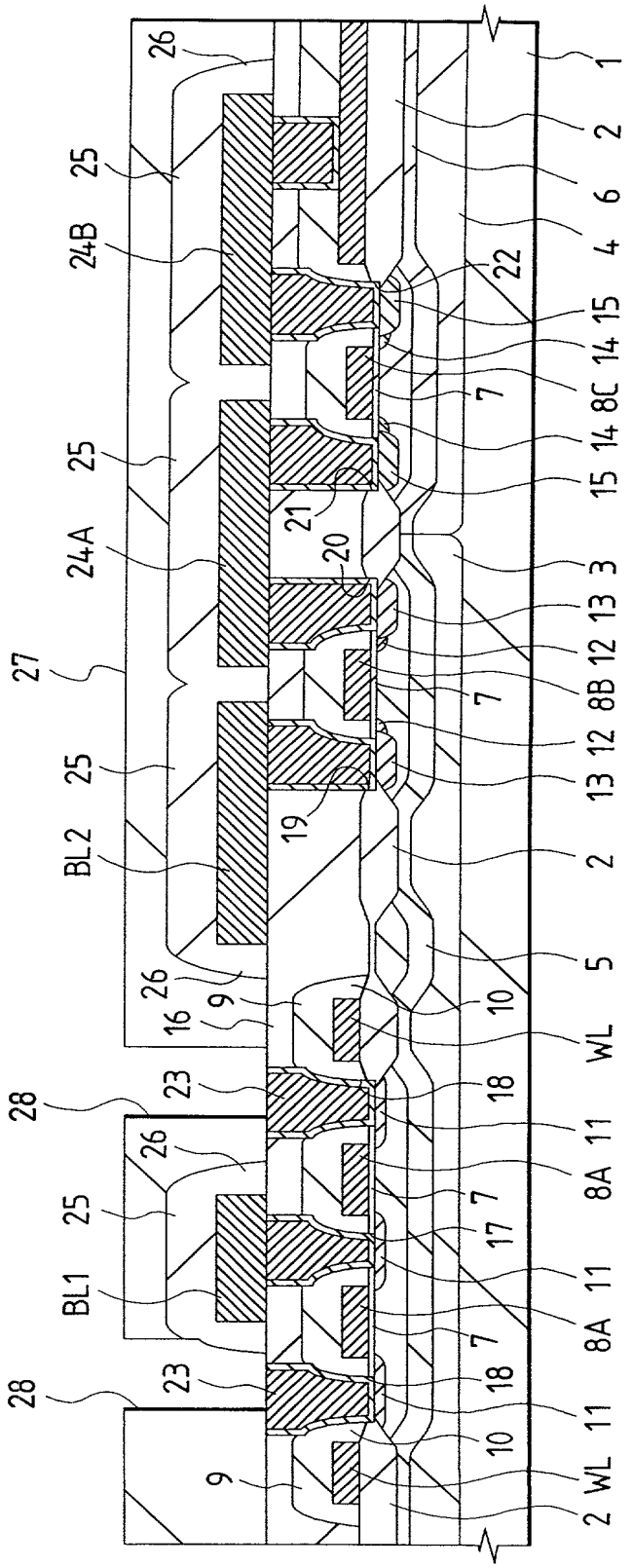
FIG. 12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WL
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8A
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17
11
8A
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18
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WL
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BL1
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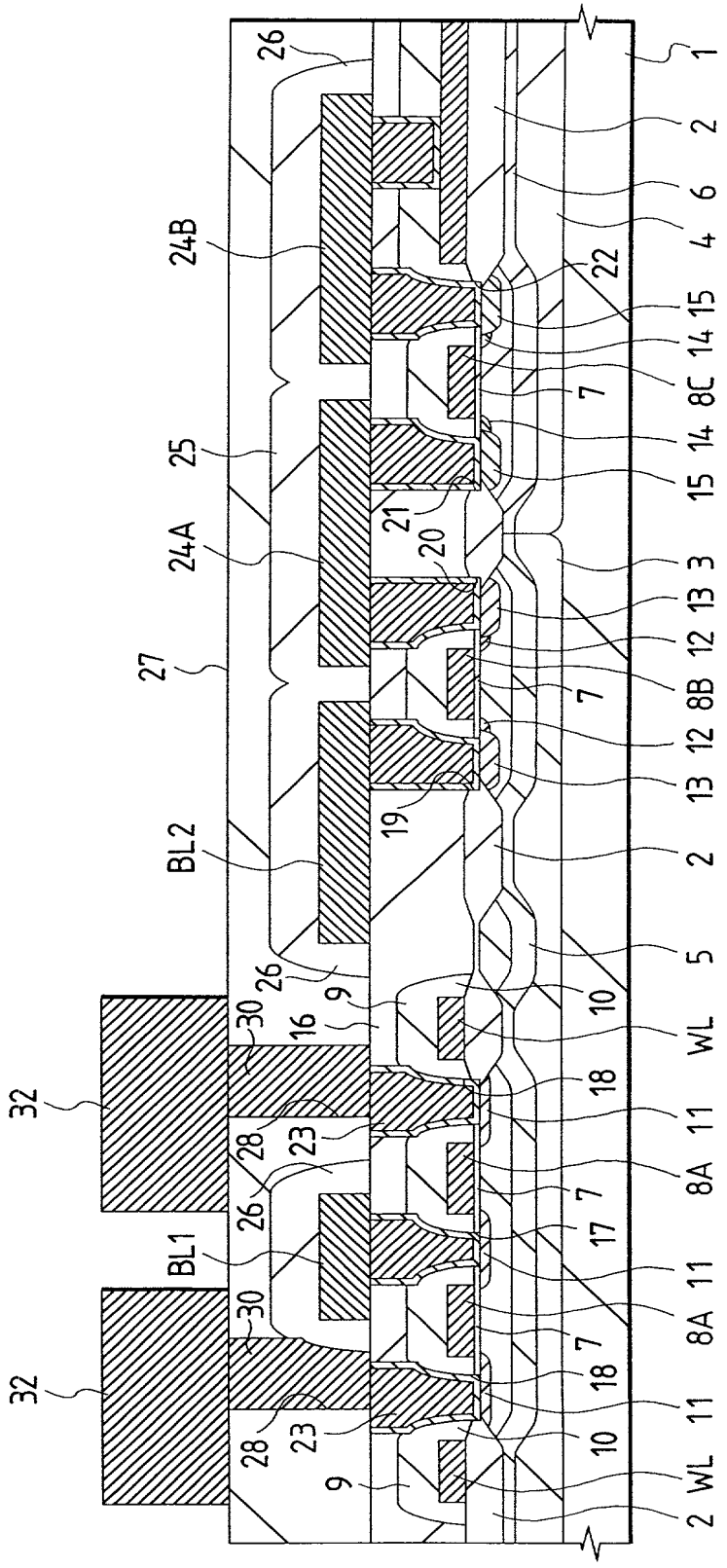
FIG. 13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WL
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8A
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8A
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WL
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BL1
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BL2
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24B
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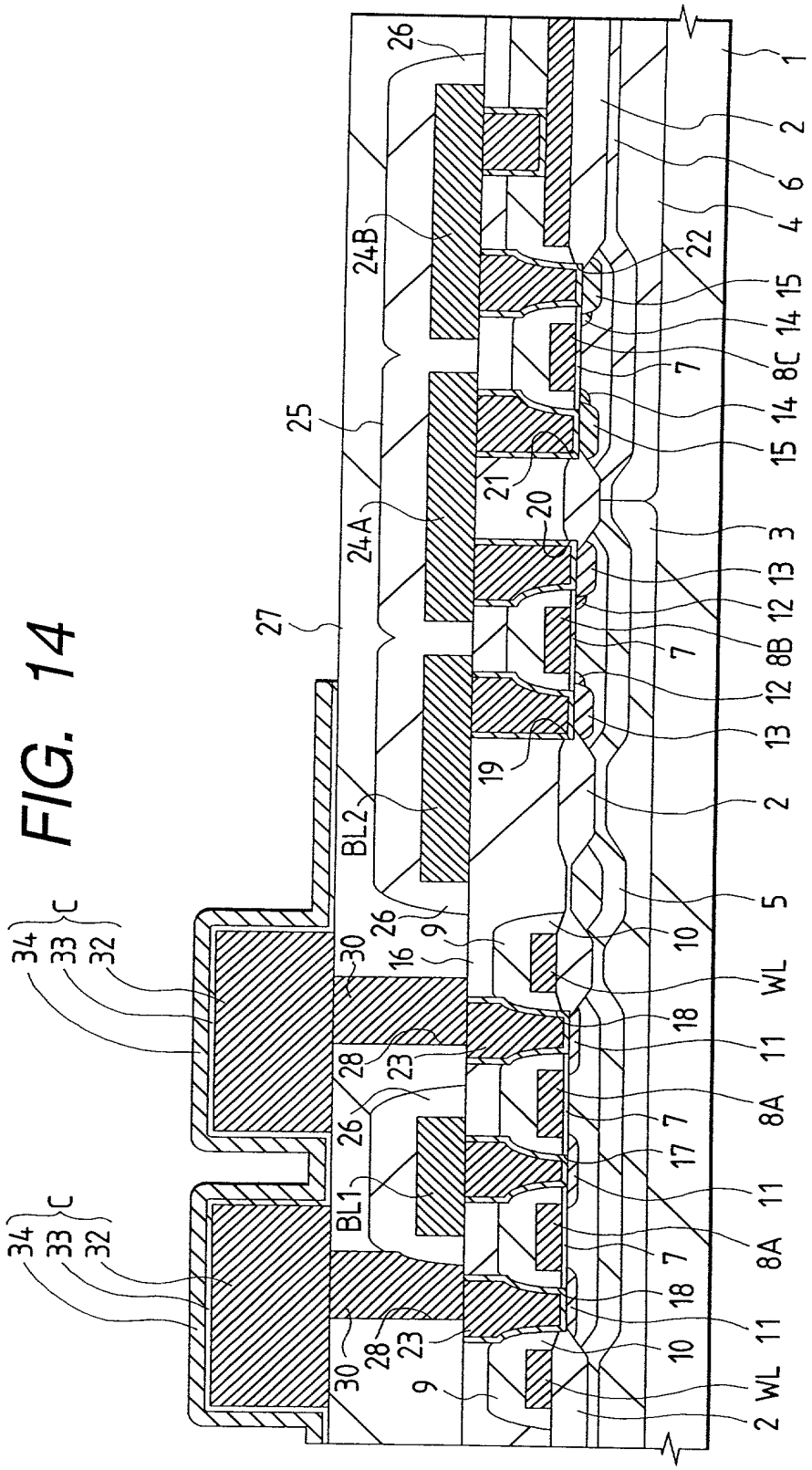
FIG. 14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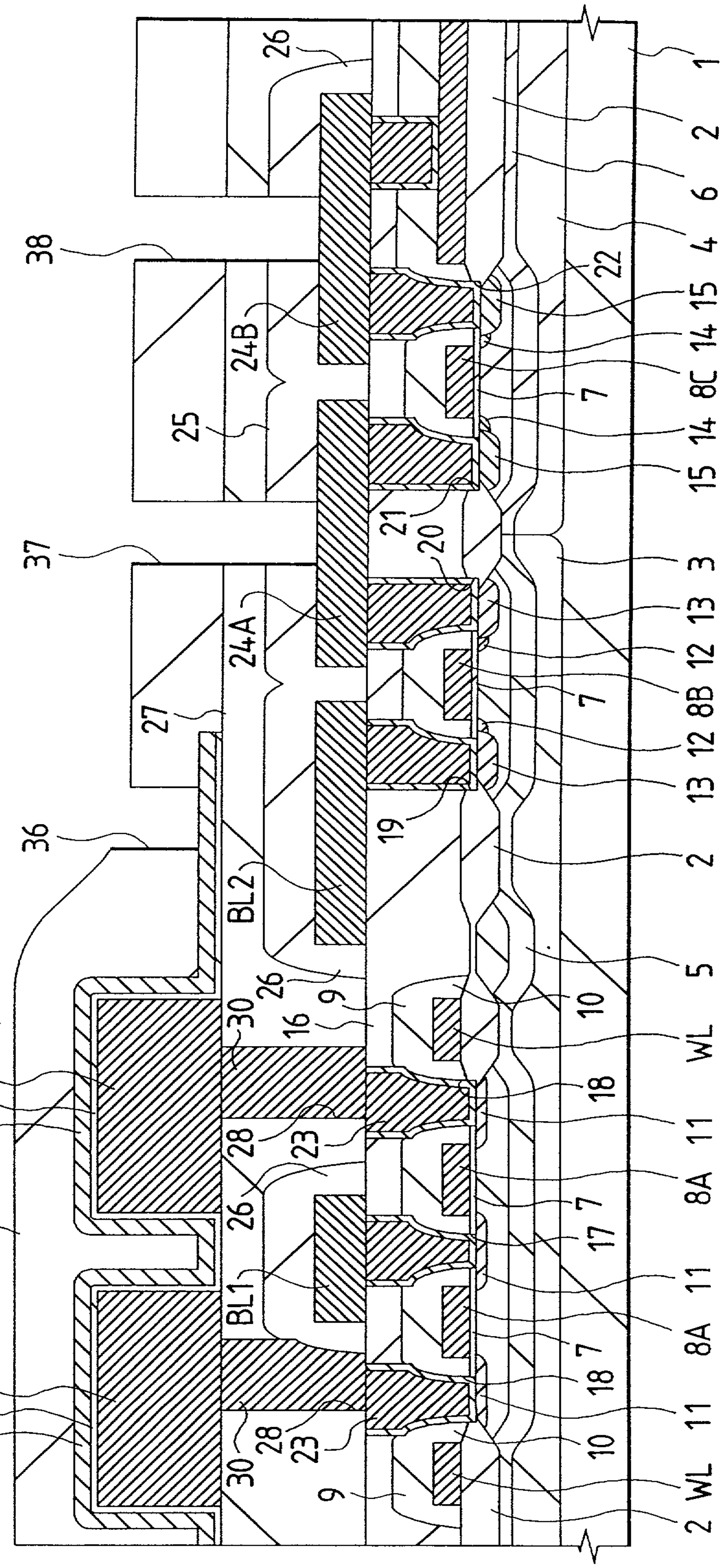
C

FIG. 15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WL
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8A
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24B
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BL2
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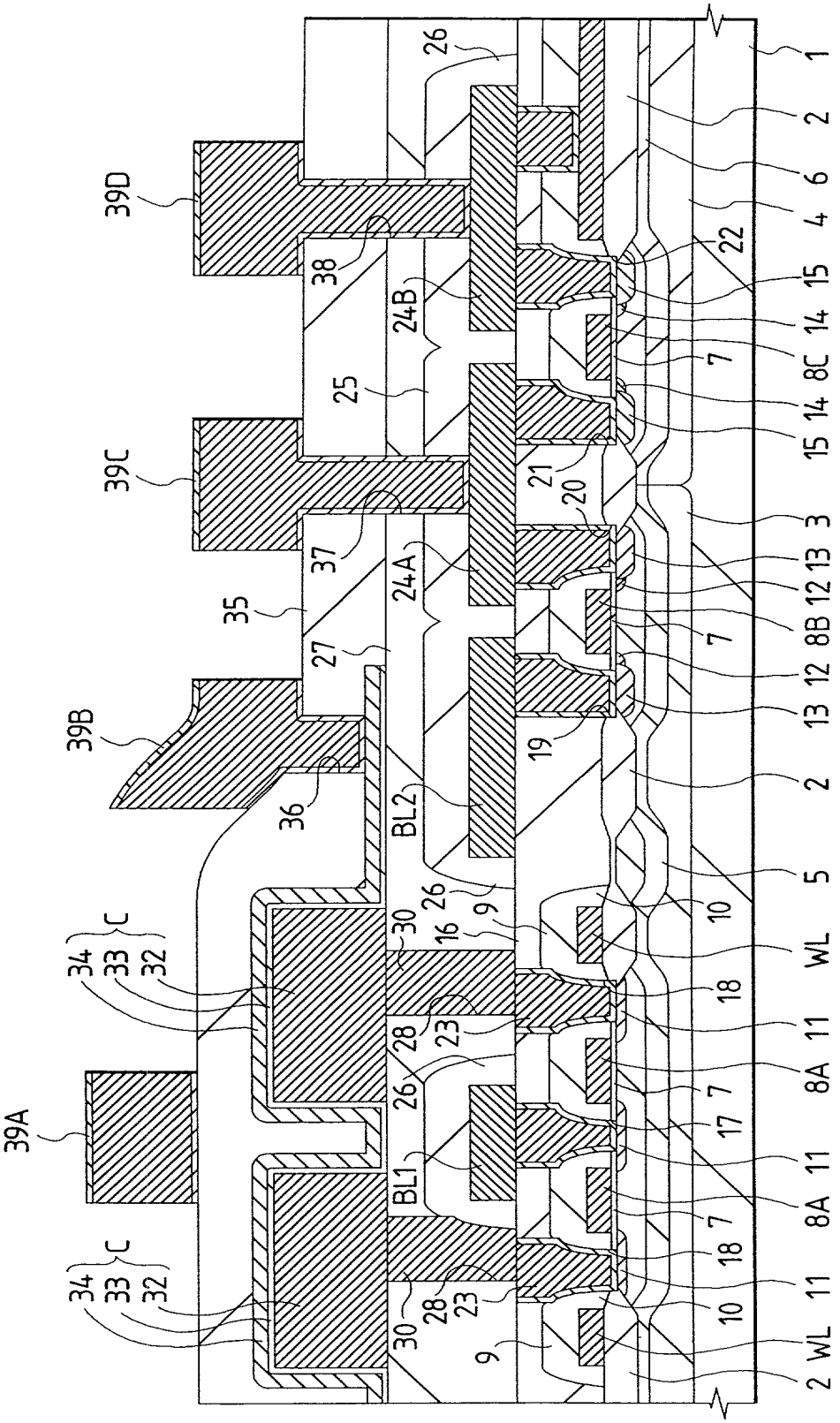
FIG. 16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BL2
WL
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FIG. 17

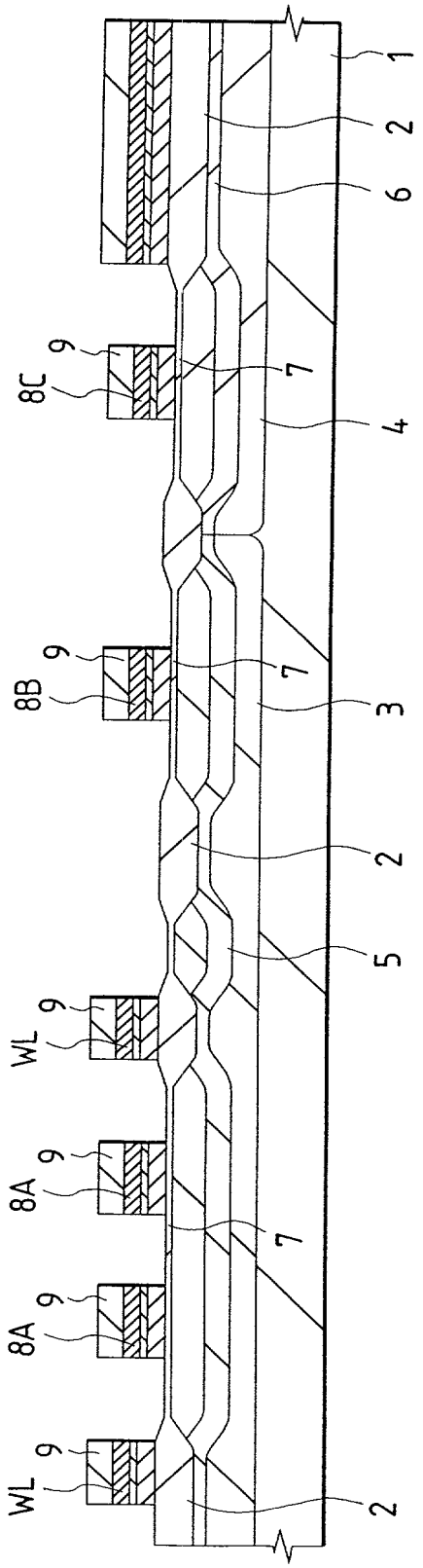
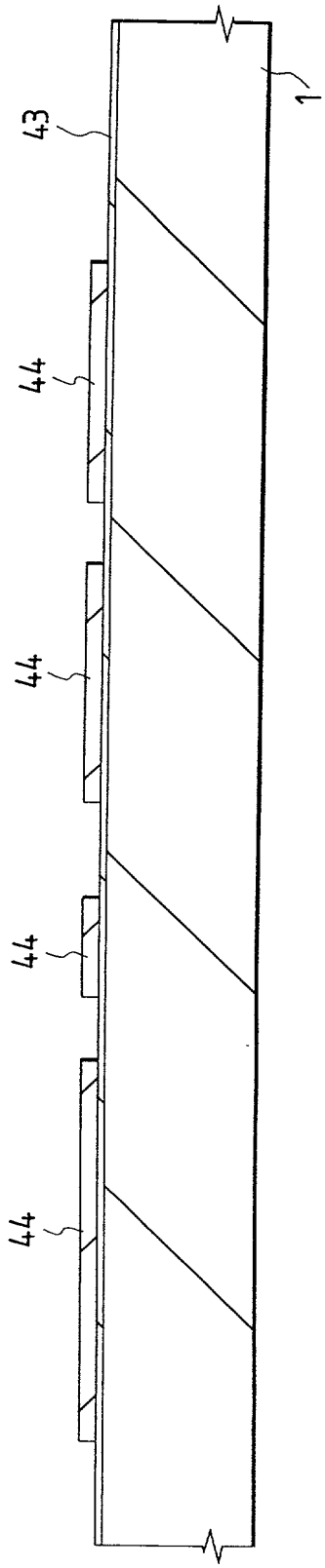


FIG. 18



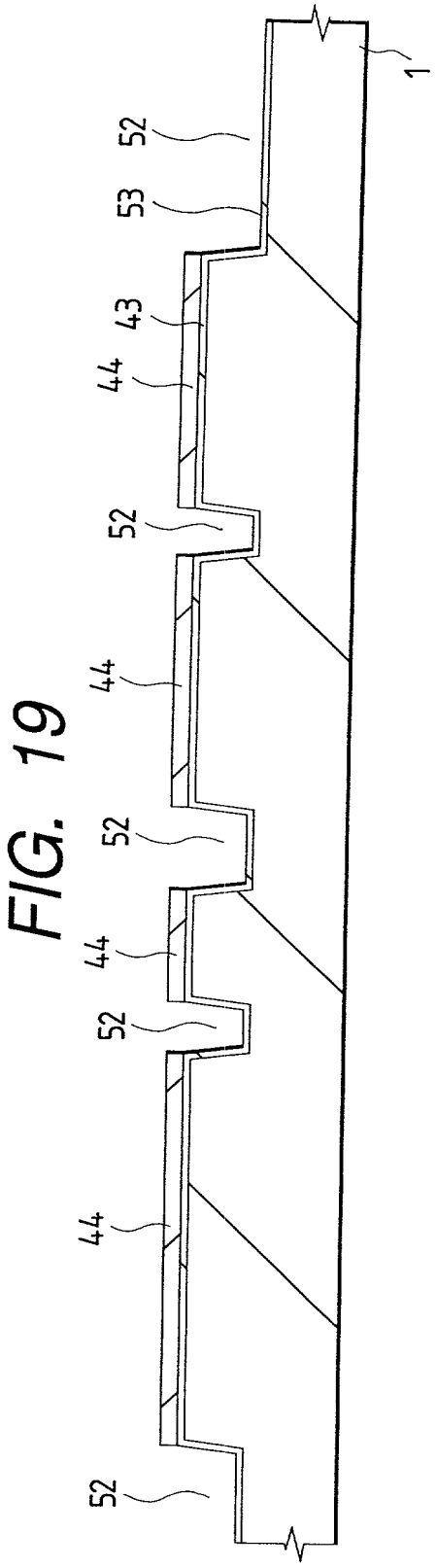


FIG. 19

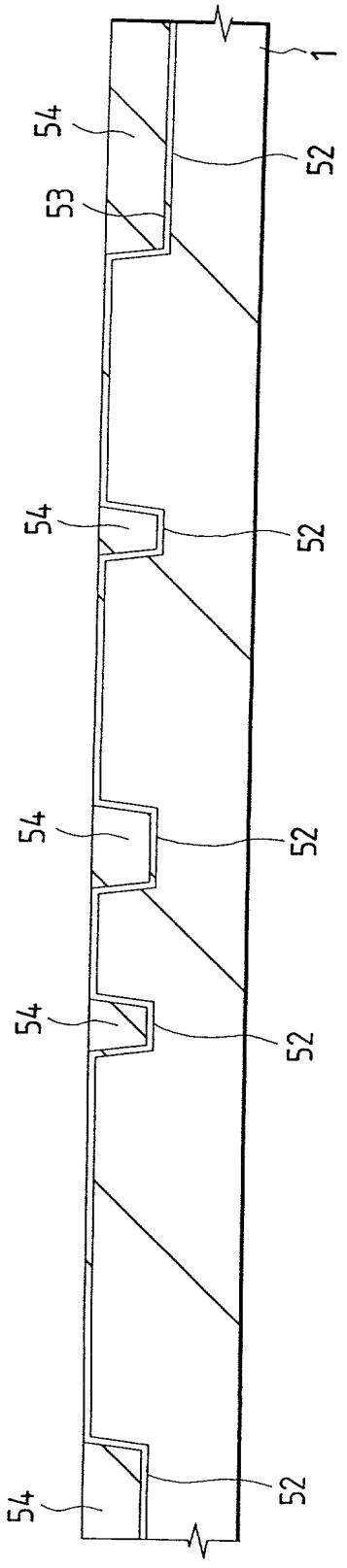


FIG. 20

FIG. 21

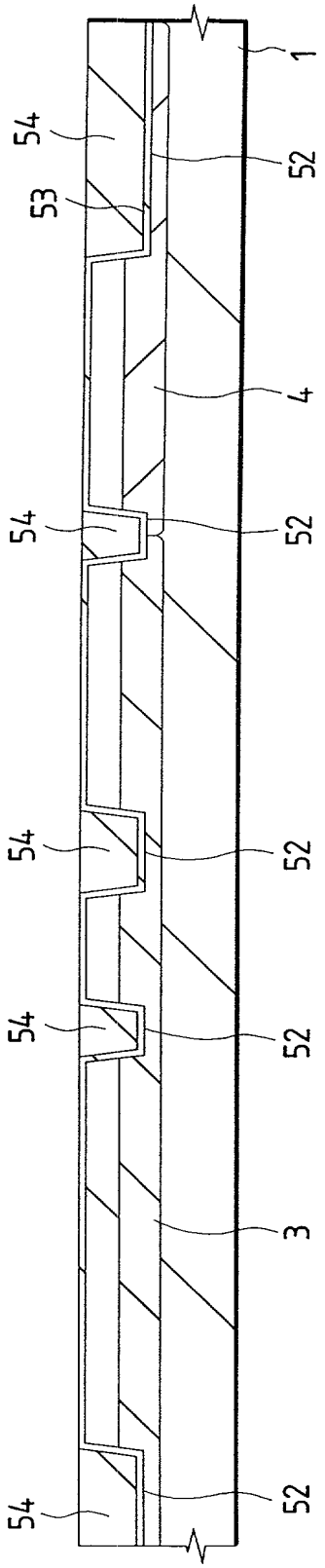

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FIG. 22

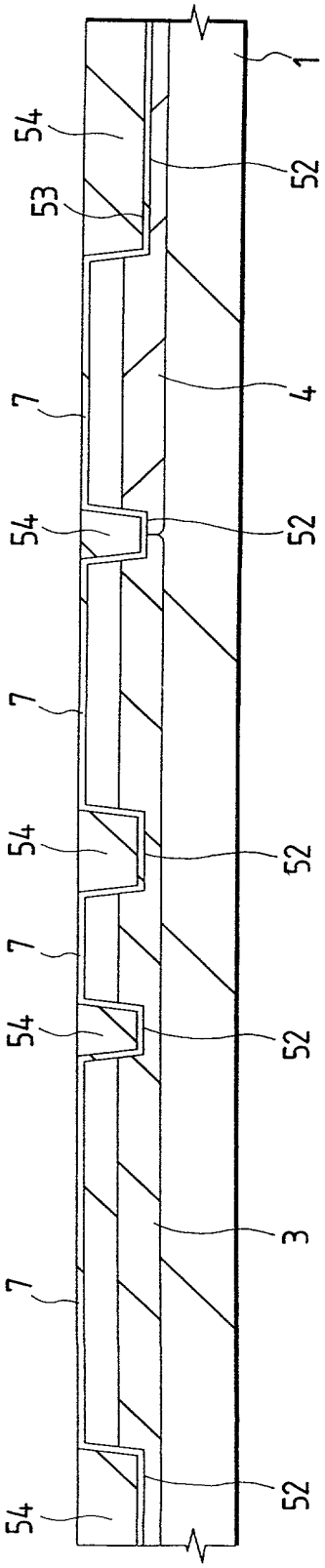
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FIG. 23

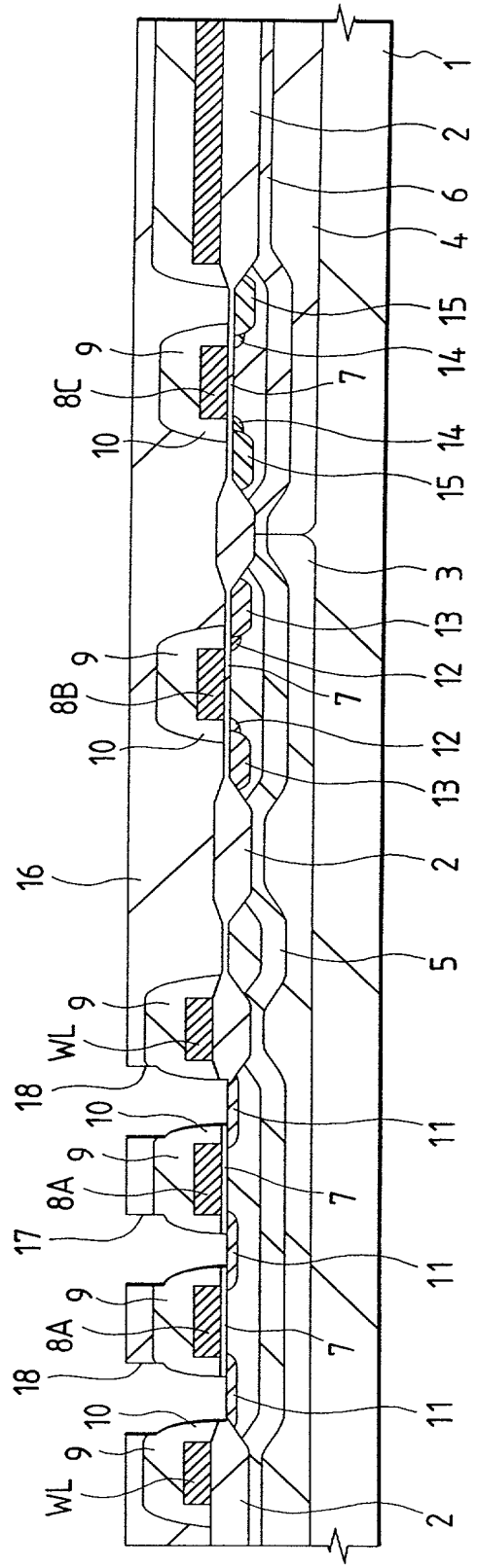
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FIG. 24

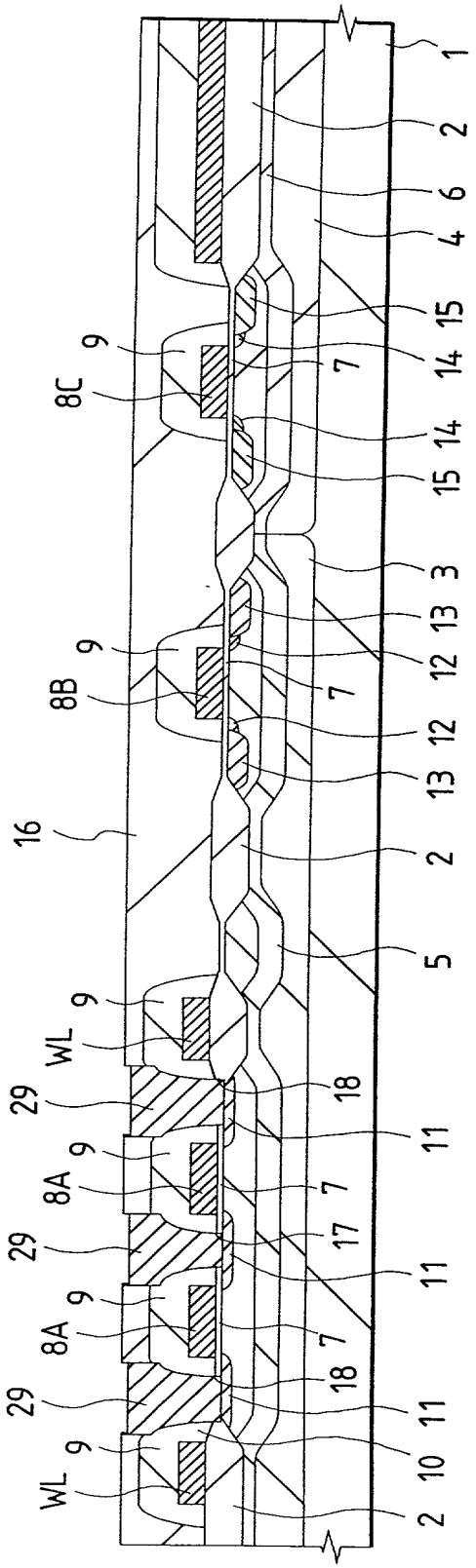
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FIG. 25

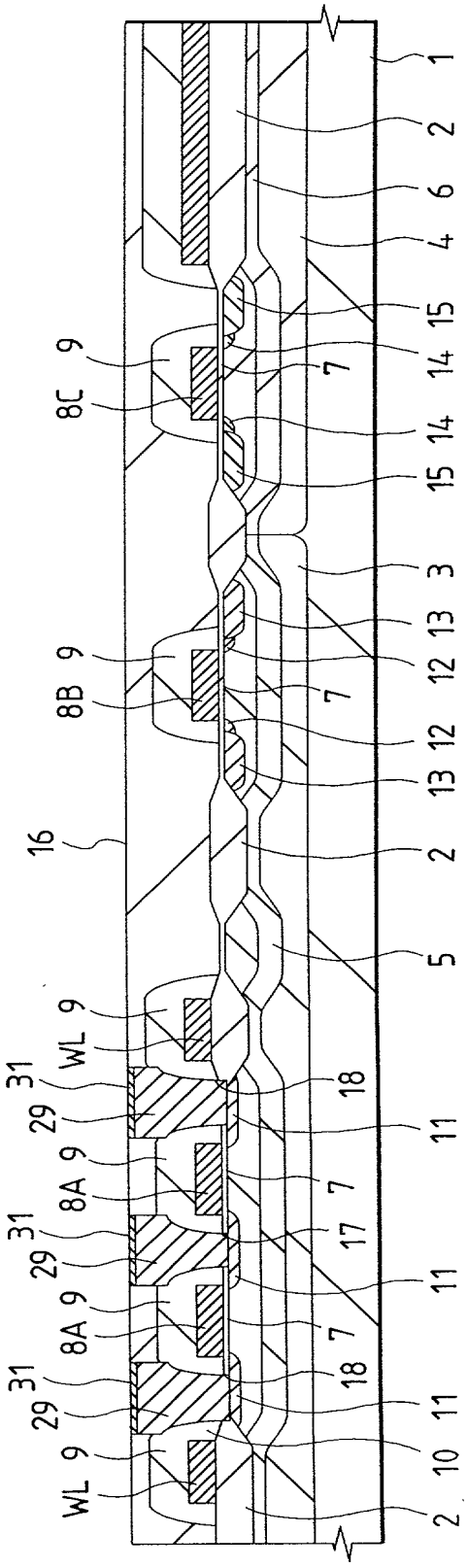
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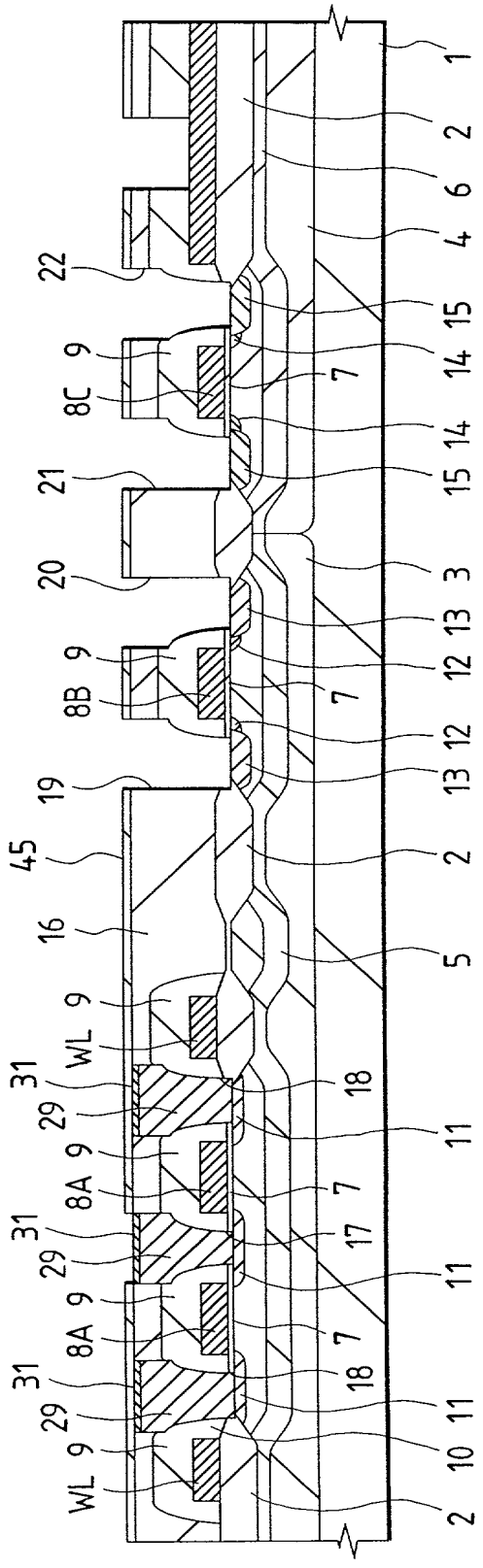
FIG. 26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WL
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FIG. 27

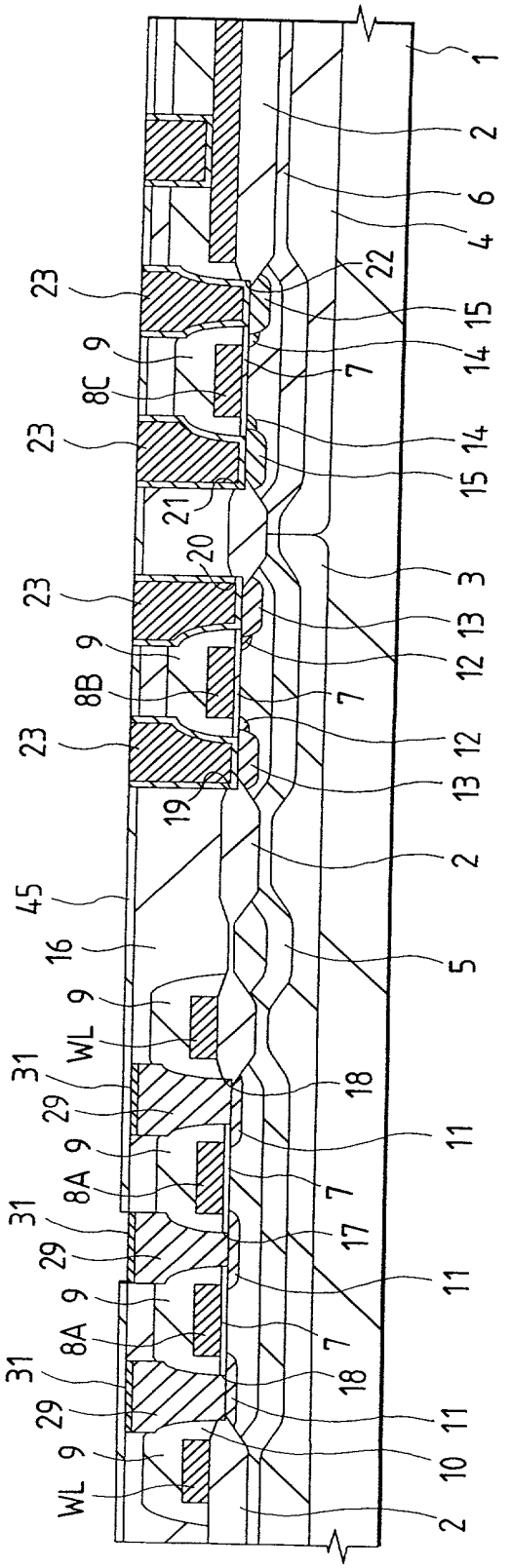
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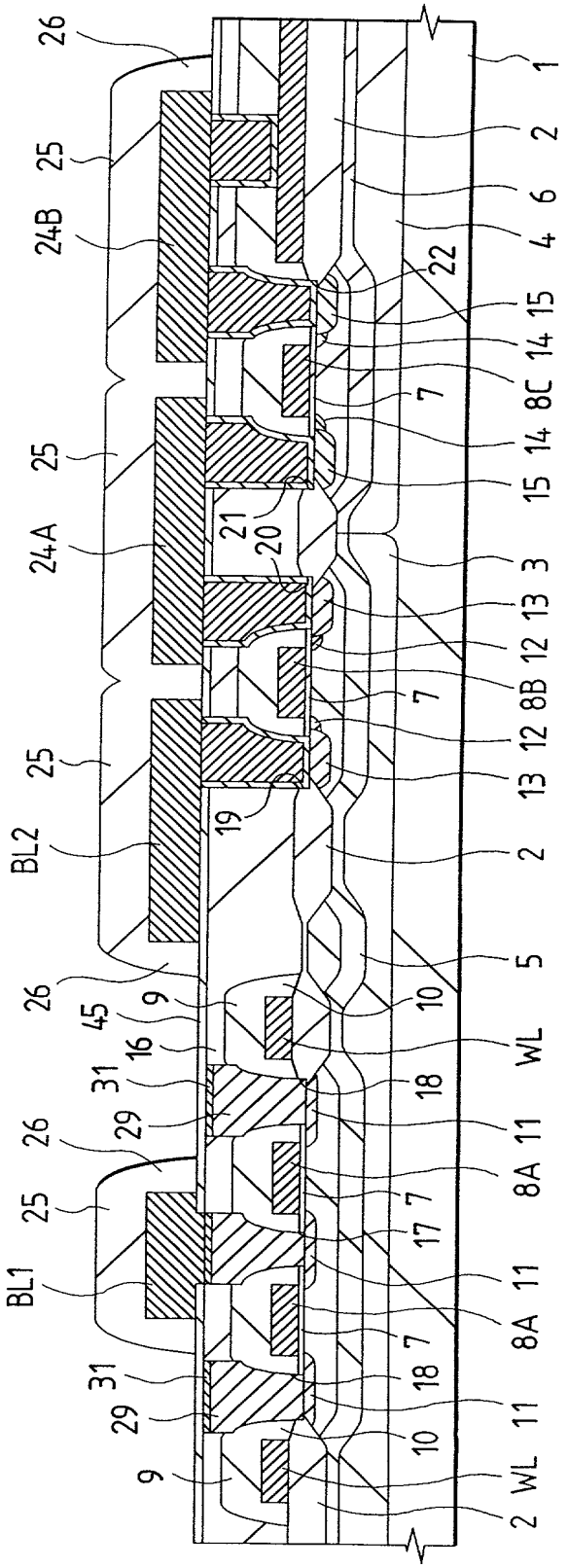
FIG. 28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24B
25
24A
25
BL2
26
45
31
29
26
25
BL1
31
29
9
2 WL 11 10 9 7 18 31 8A 11 17 7 18 29 11 WL 16 9 10 5 2 13 19 12 8B 7 13 12 3 20 21 14 15 8C 7 14 15 22 4 6 2 1

FIG. 29

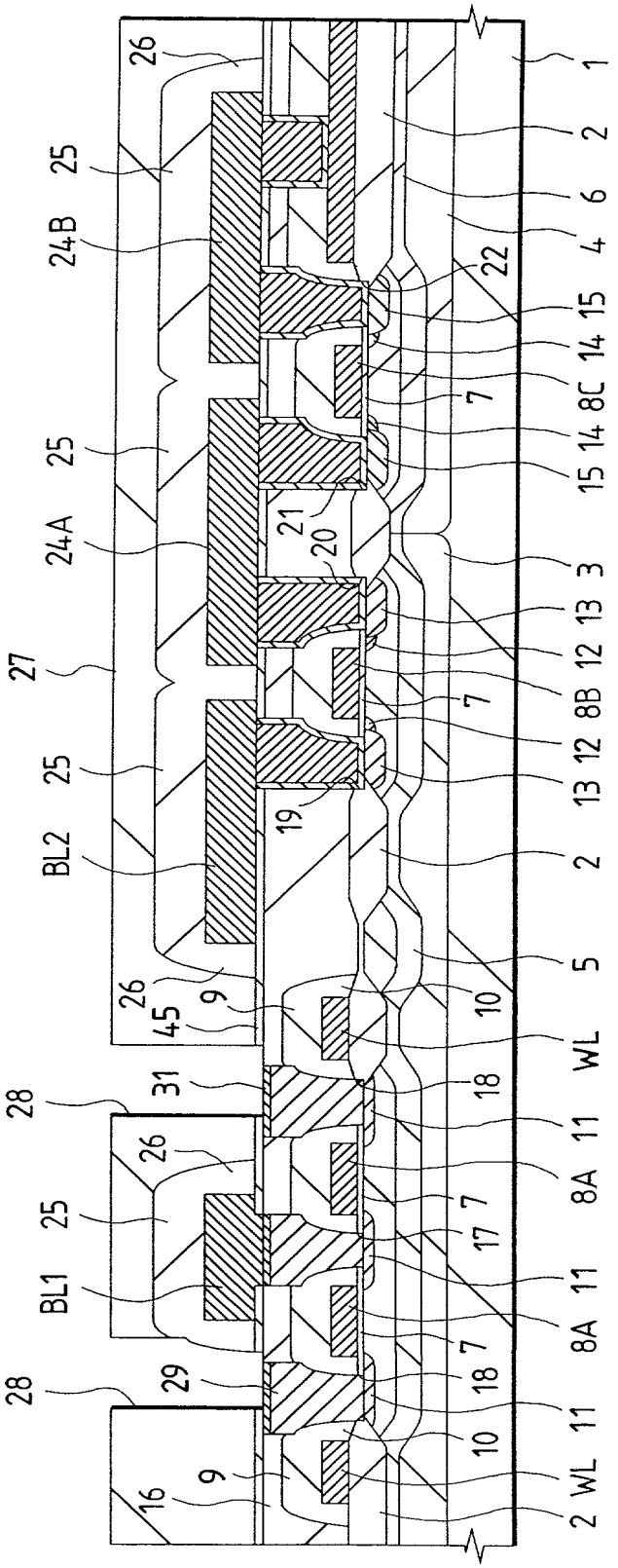

1
2
6
4
22
15
14
8C
7
14
15
3
13
12
8B
7
12
13
2
5
10
WL
18
11
8A
7
17
11
8A
7
18
11
10
WL
2
16
9
29
28
BL1
25
26
31
28
45
9
26
BL2
25
19
27
24A
25
21
20
24B
25
26

FIG. 30

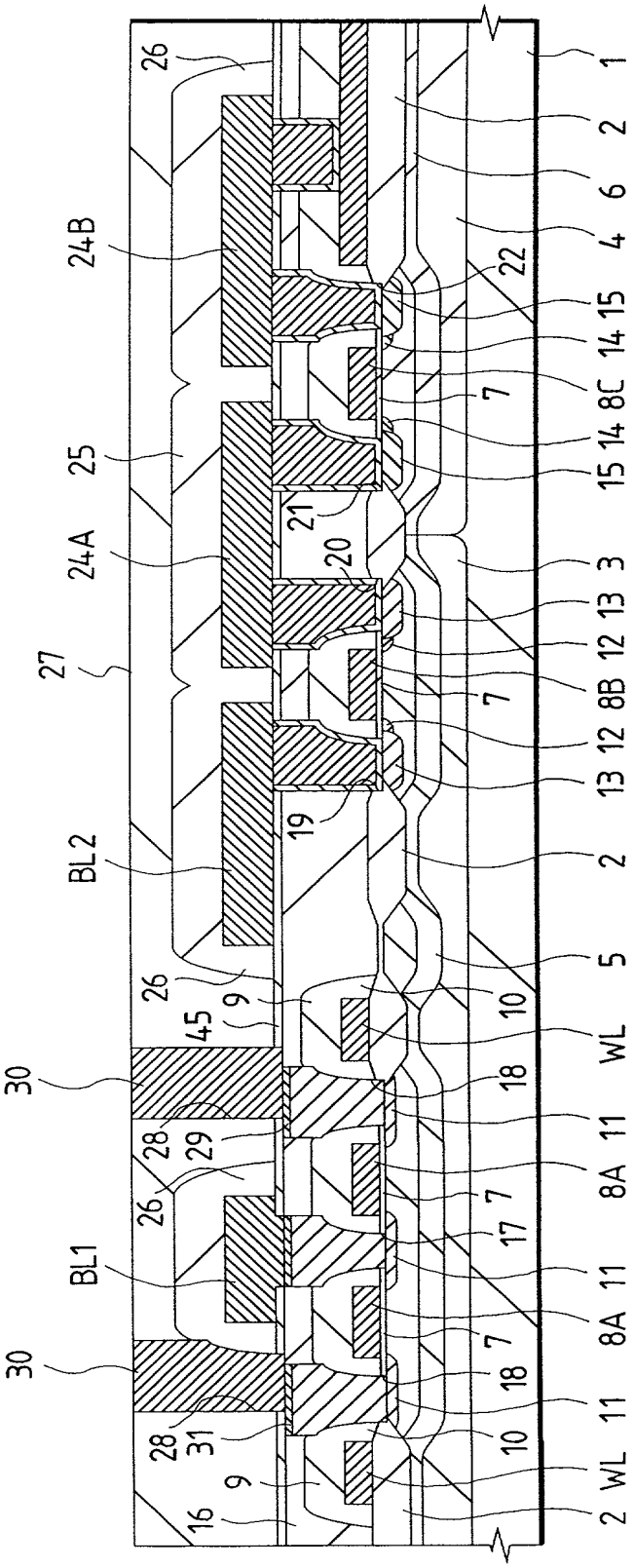

26
24B
25
24A
27
BL2
30
BL1
30
26
45
9
28
29
26
28
31
9
16
2 WL 11 8A 11 7 18 10 WL 5 2 13 12 8B 12 13 3 15 14 8C 14 15 4 6 2 1
22
7
21
20
19
18
17
10

FIG. 31

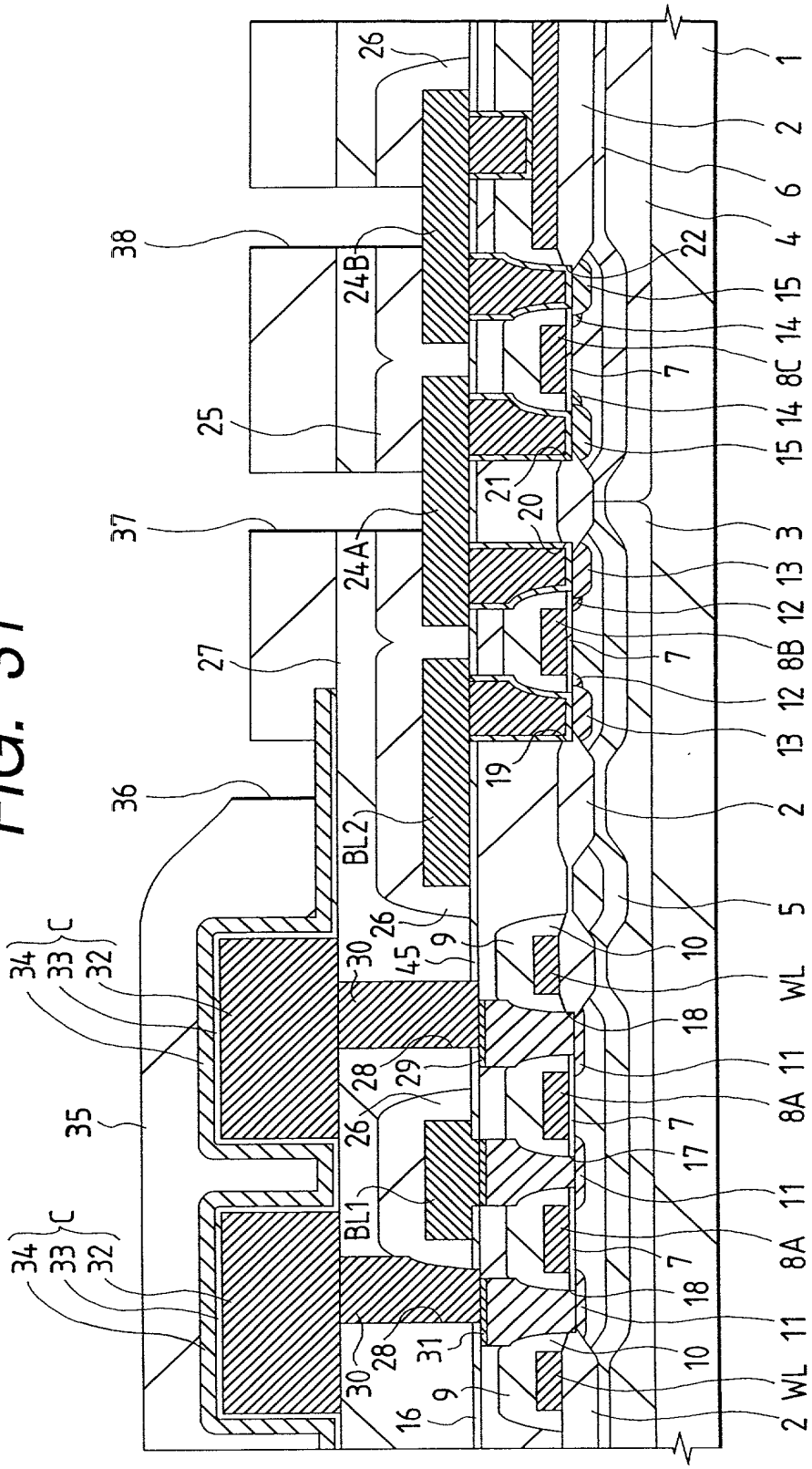

1
2
6
4
22
15
14
8C
7
14
15
3
13
12
8B
7
12
13
2
5
10
WL
18
11
8A
7
17
11
8A
7
18
10
11
WL
2
16
9
30
28
31
BL1
26
28
29
7
35
34
33
32
C
34
33
32
C
30
45
9
26
BL2
36
27
37
24A
19
21
20
25
38
24B
26

FIG. 32

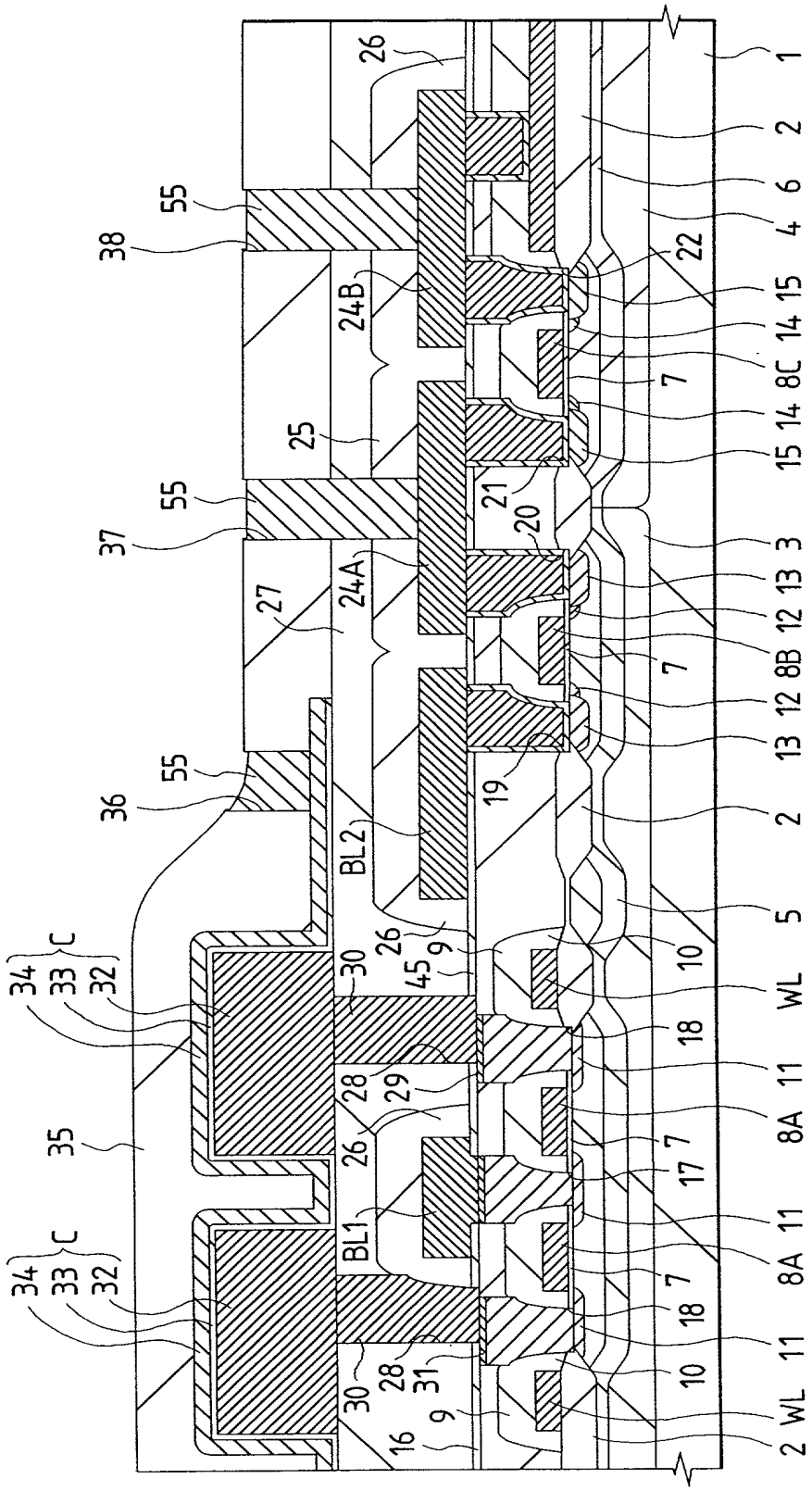

1
2
6
4
22
15
14
8C
7
15
14
21
20
3
13
12
8B
7
12
13
19
2
5
10
WL
18
11
8A
7
17
11
8A
7
18
11
10
WL
2
26
55
38
24B
25
55
37
27
24A
55
36
BL2
26
9
45
30
34
33
32
C
35
28
29
26
BL1
34
33
32
C
30
28
31
9
16

FIG. 33

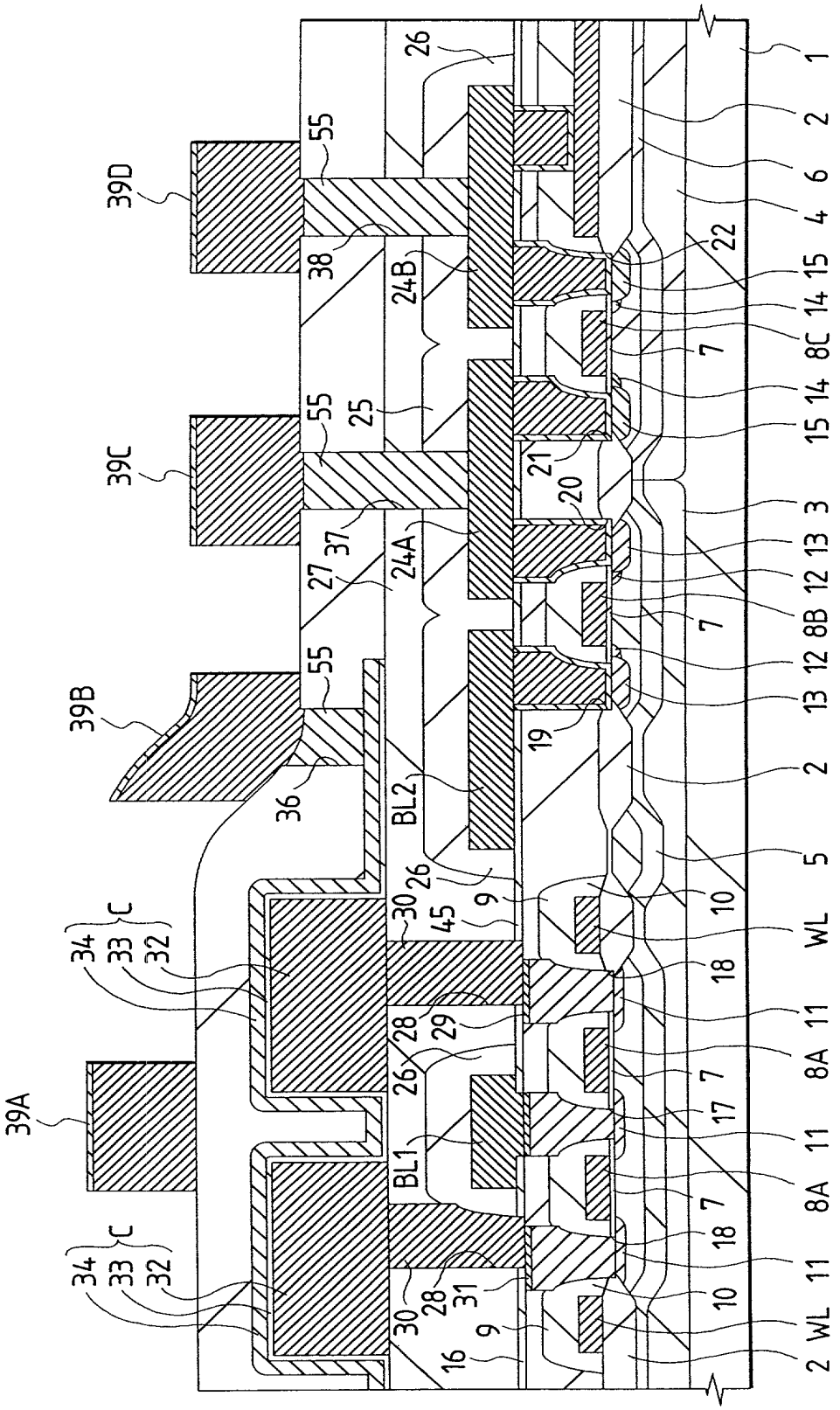

39A
39B
39C
39D
34
33
32
C
55
38
24B
25
27
24A
37
36
BL2
BL1
26
30
45
9
28
29
31
16
WL
2
5
10
18
11
8A
7
17
12
8B
13
3
20
21
14
8C
15
22
4
6
1

FIG. 34

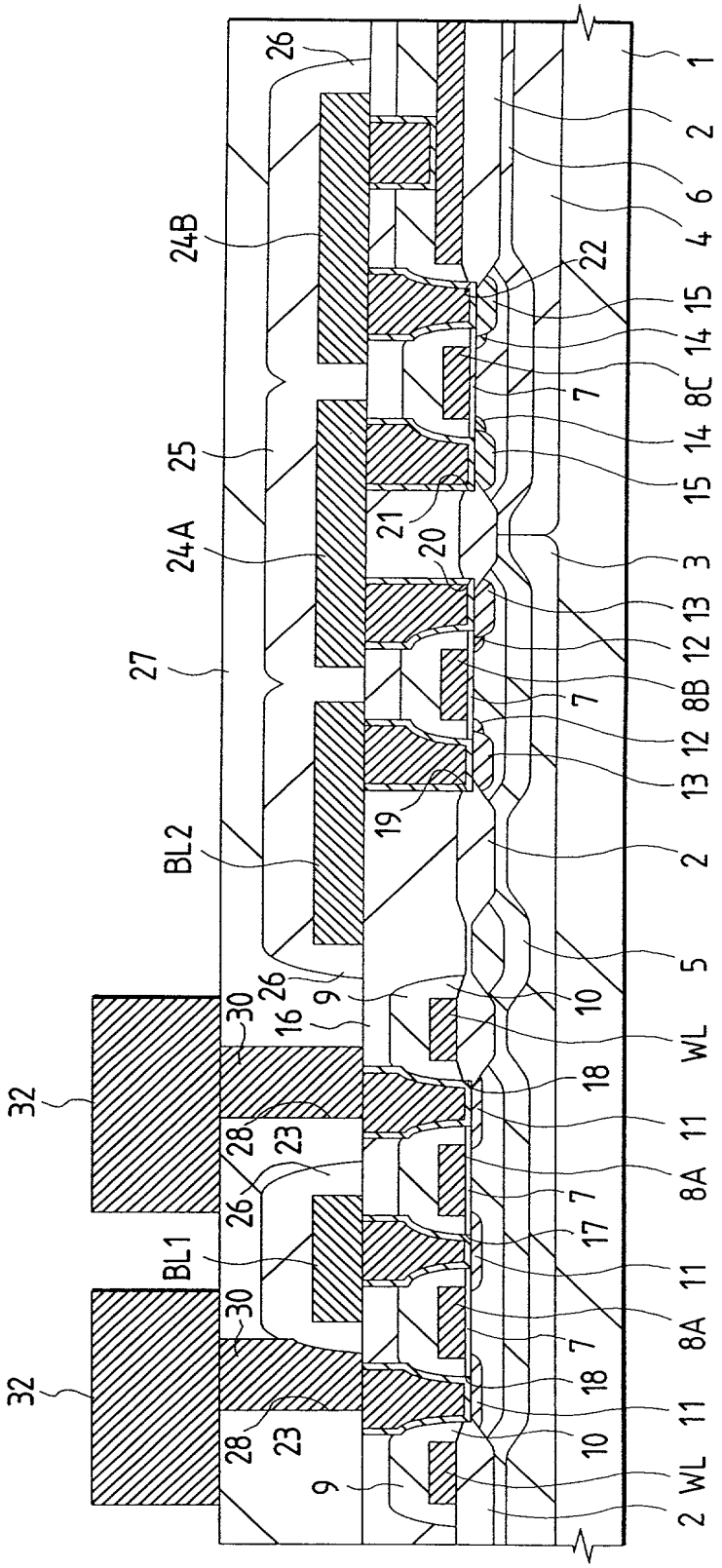

1
2
6
4
22
15
14
8C
7
14
15
3
13
12
8B
7
12
13
2
5
10
WL
18
11
8A
7
17
11
8A
7
18
11
10
WL
2
9
23
28
32
BL1
30
16
26
9
19
BL2
27
24A
25
21
20
24B
26

FIG. 35

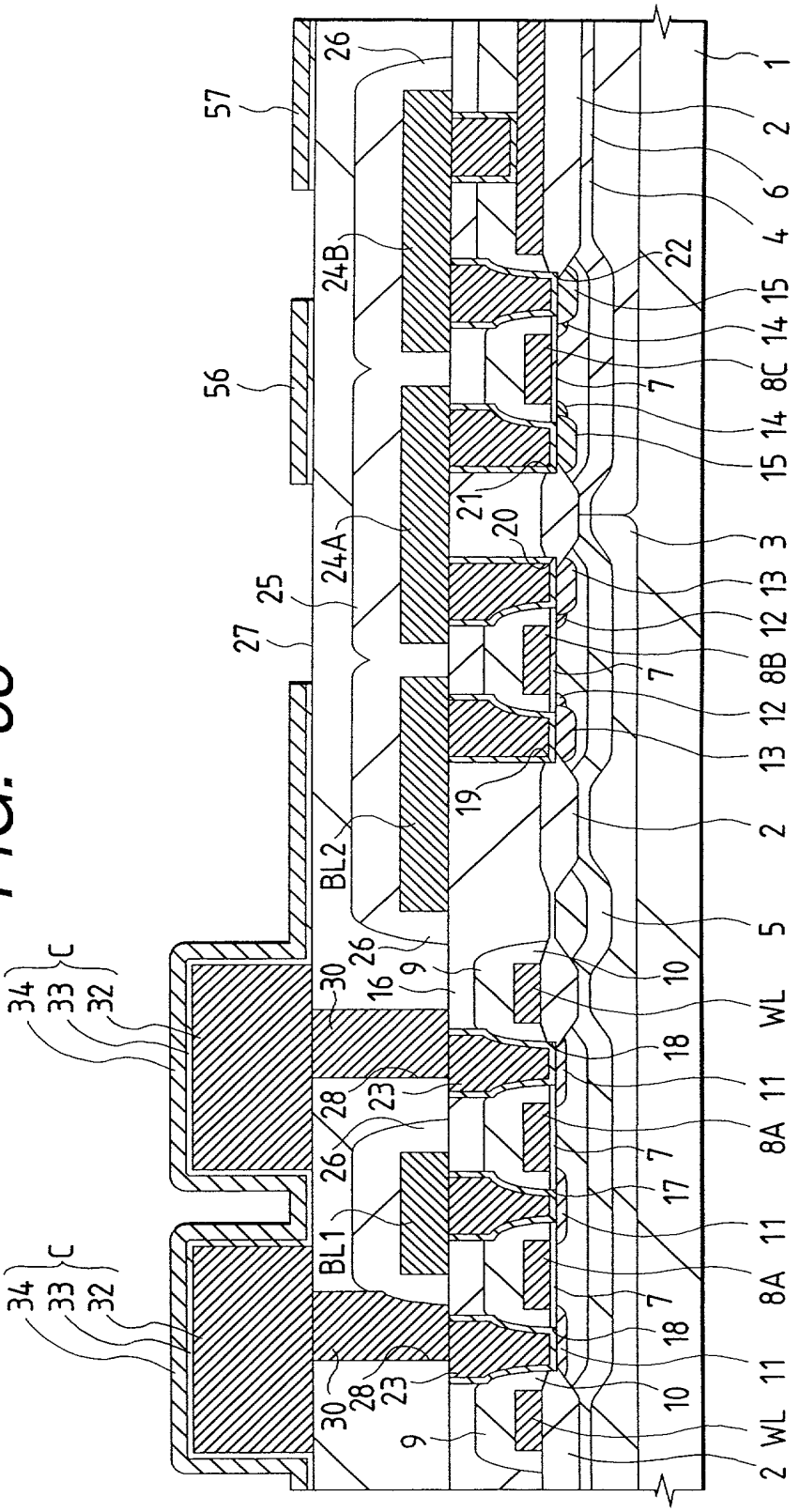

57
56
25
27
24A
24B
BL1
BL2
WL
C
34
33
32
30
28
23
26
16
9
19
21
20
22
15
14
8C
12
13
8B
11
8A
18
17
10
7
5
4
6
3
2
1

FIG. 36

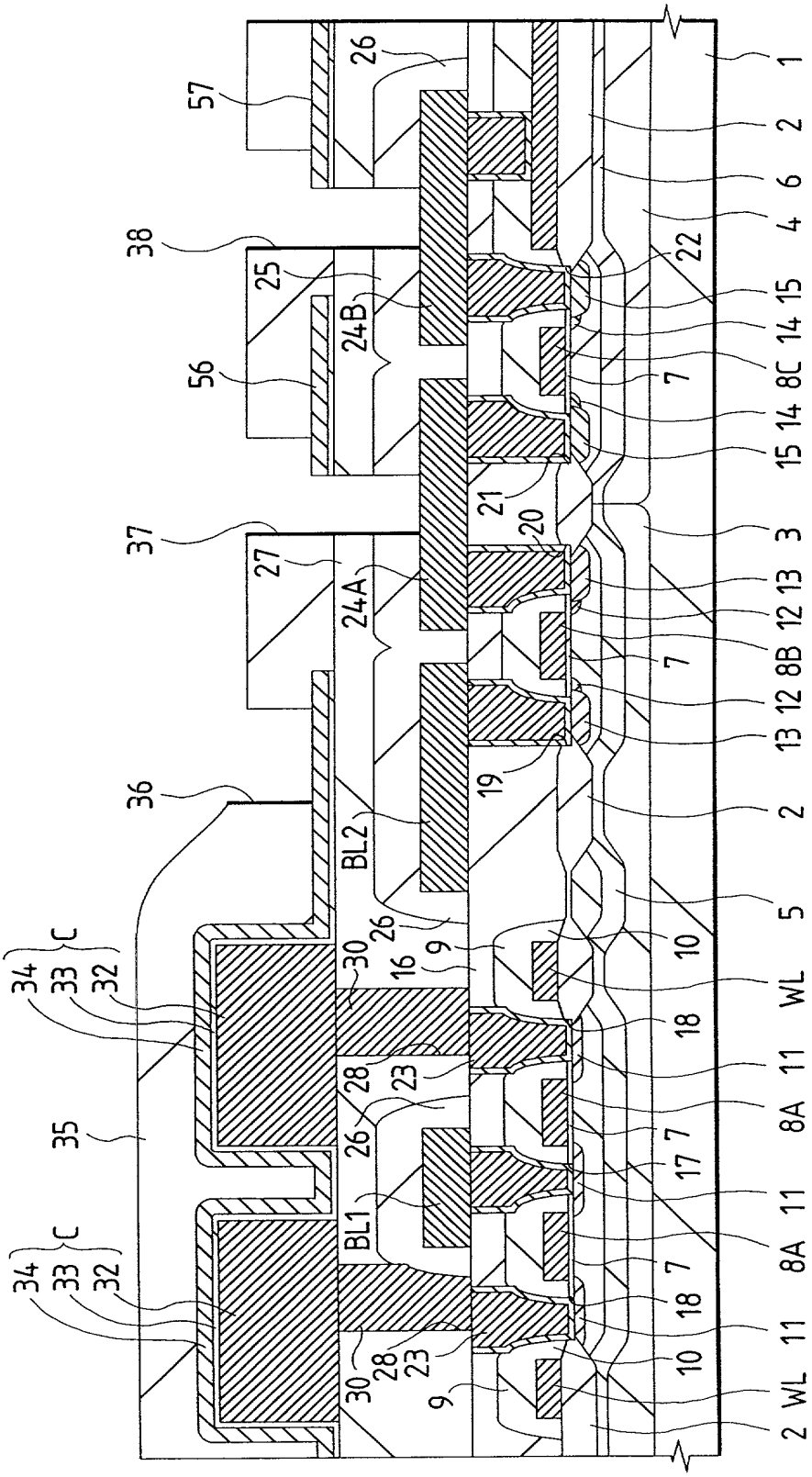

57
26
1
38
25
22
2
6
56
24B
4
15
14
7
8C
21
20
15
14
37
27
3
24A
13
12
7
8B
19
13
12
36
BL2
2
5
34
33
32
C
30
26
9
16
10
WL
18
28
23
11
8A
35
26
7
17
BL1
11
8A
34
33
32
C
7
18
28
23
10
11
WL
30
9
2

FIG. 37

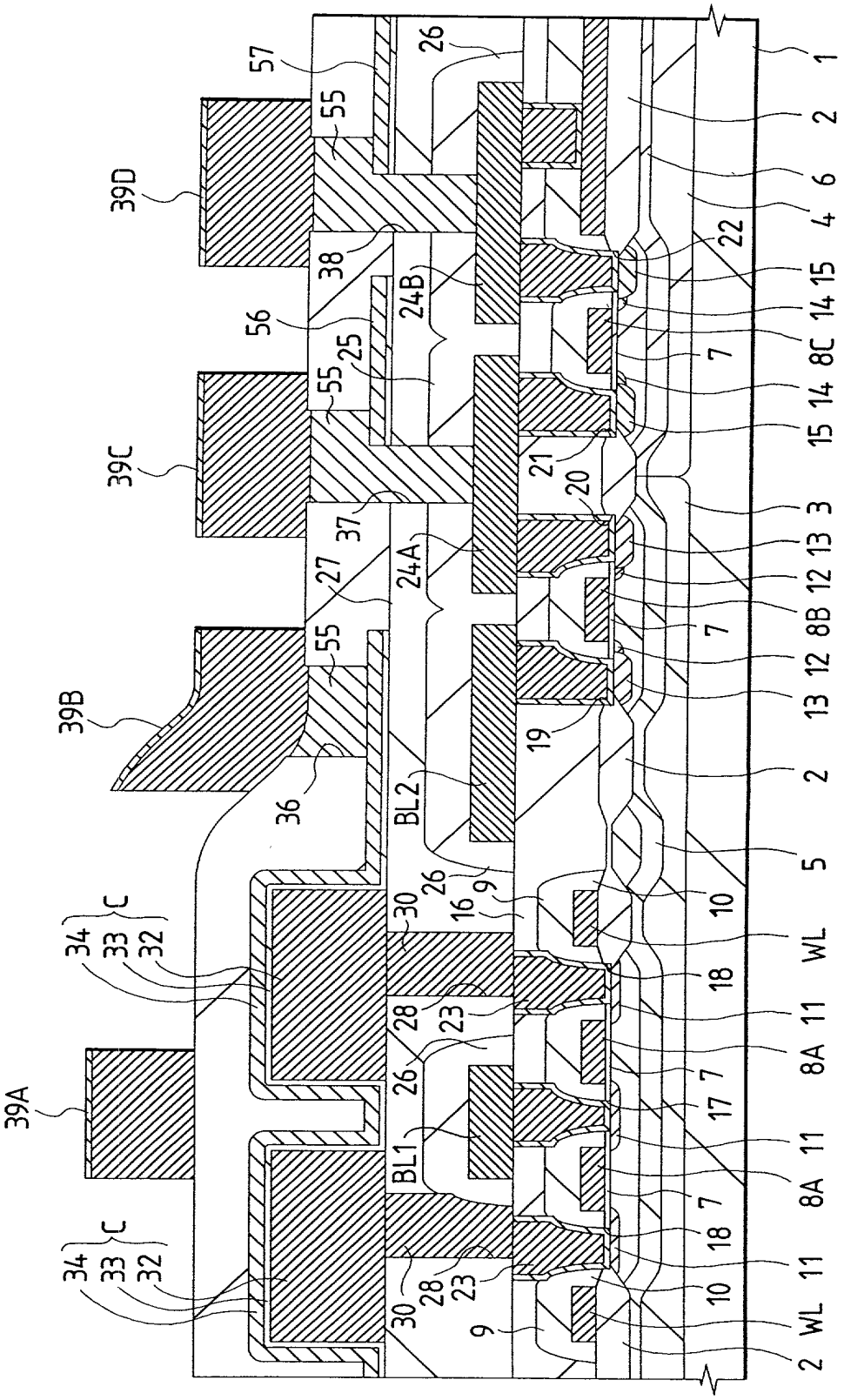

39A
39B
39C
39D
BL1
BL2
WL
34
33
32
C
36
37
38
55
56
57
24A
24B
25
26
27
28
30
23
16
9
10
11
18
17
7
8A
8B
8C
19
20
21
22
12
13
14
15
3
4
6
1
2
5

FIG. 38

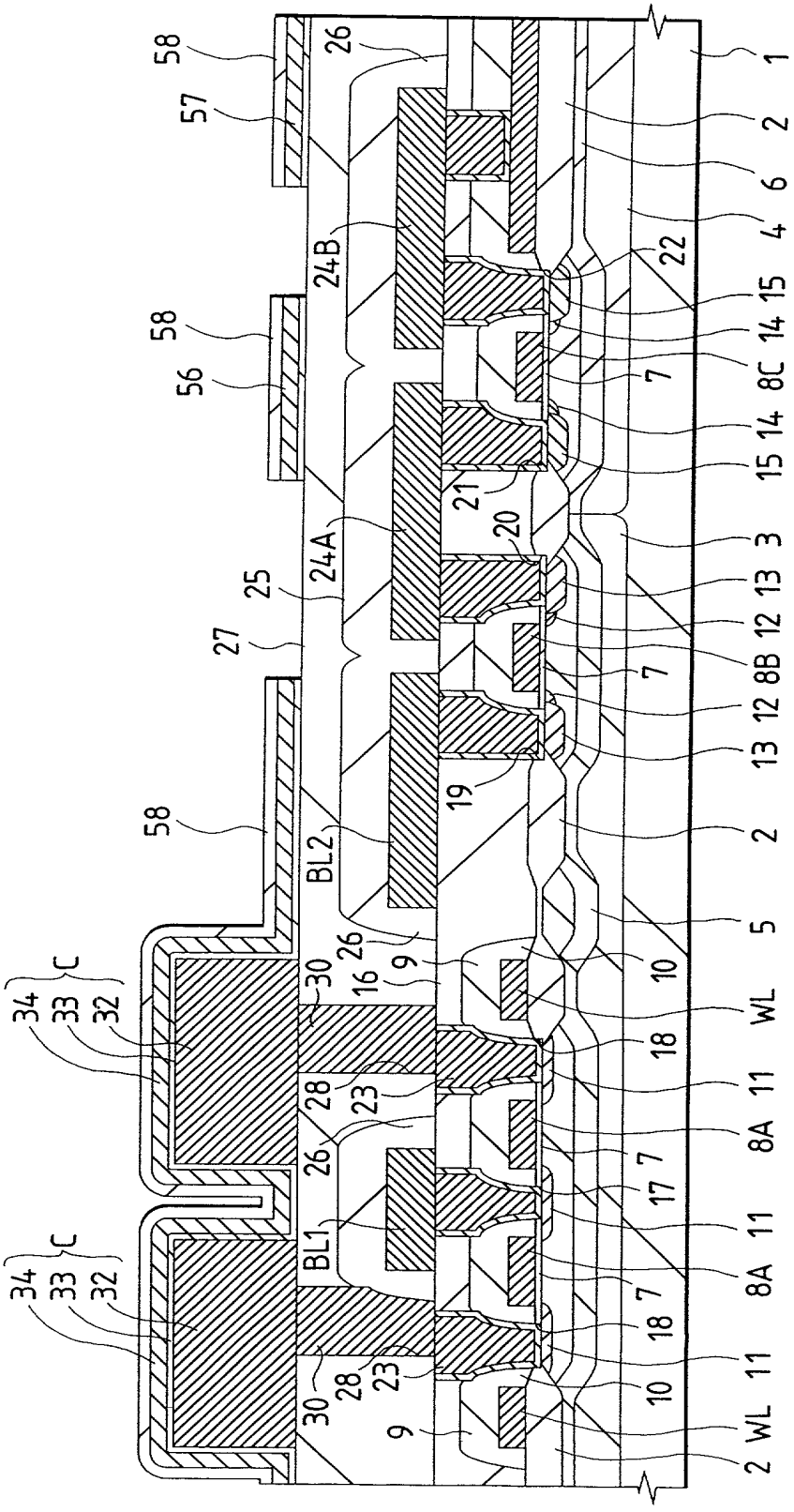

58
57
56
58
58
27
25
24A
24B
26
1
2
6
4
22
15
14
8C
7
15
14
21
20
3
13
12
8B
7
13
12
19
2
BL2
5
10
WL
18
11
8A
7
17
11
8A
7
18
11
10
WL
2
9
30
28
23
26
16
34
33
32
C
BL1

FIG. 39

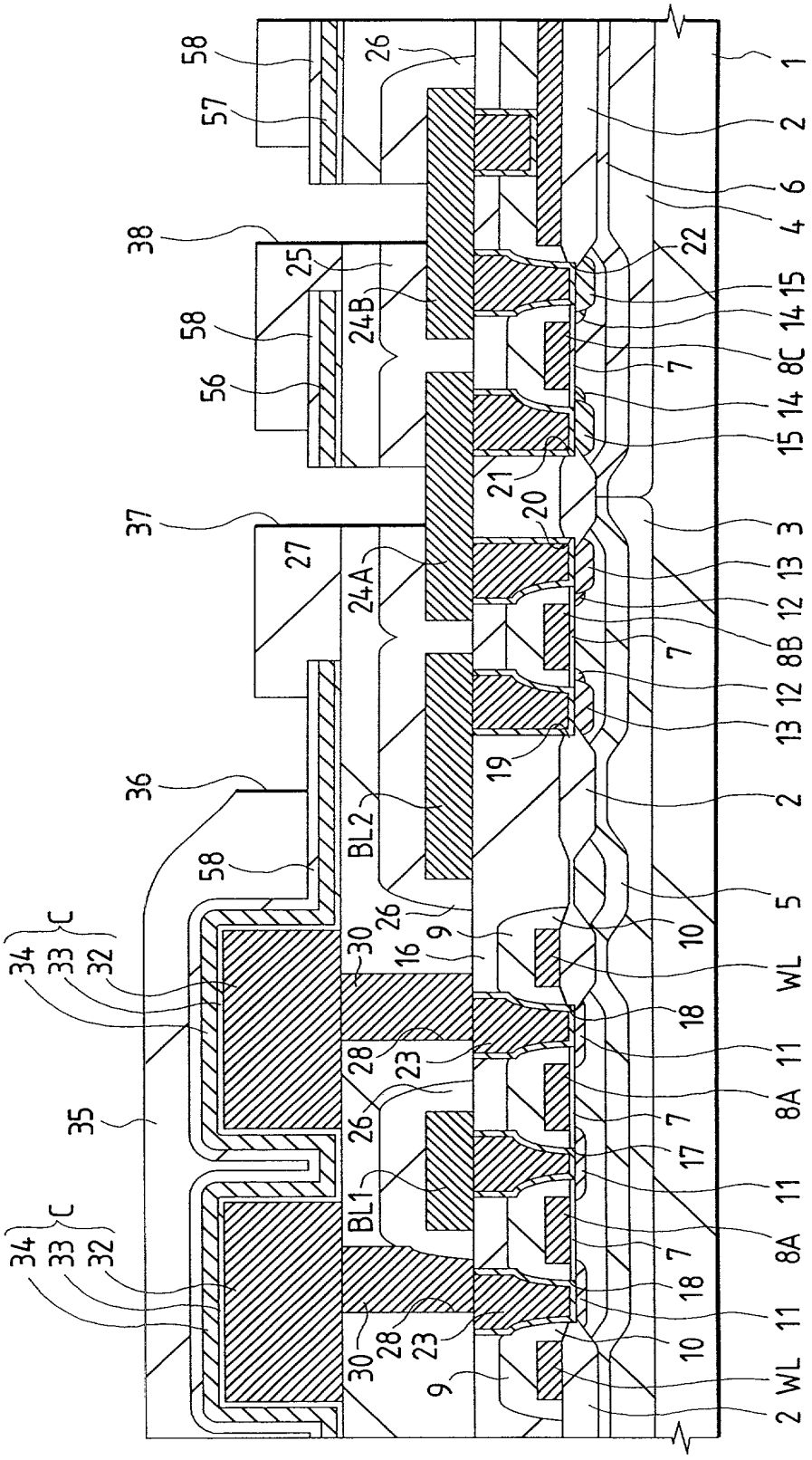

58
57
26
1
2
38
25
22
6
4
58
24B
56
7
8C
14
15
37
27
21
20
3
24A
13
12
7
8B
36
BL2
19
58
34
33
32
C
30
26
9
16
10
5
35
28
23
18
WL
11
26
7
8A
BL1
17
11
34
33
32
C
7
18
8A
30
28
23
10
11
9
WL
2

FIG. 40

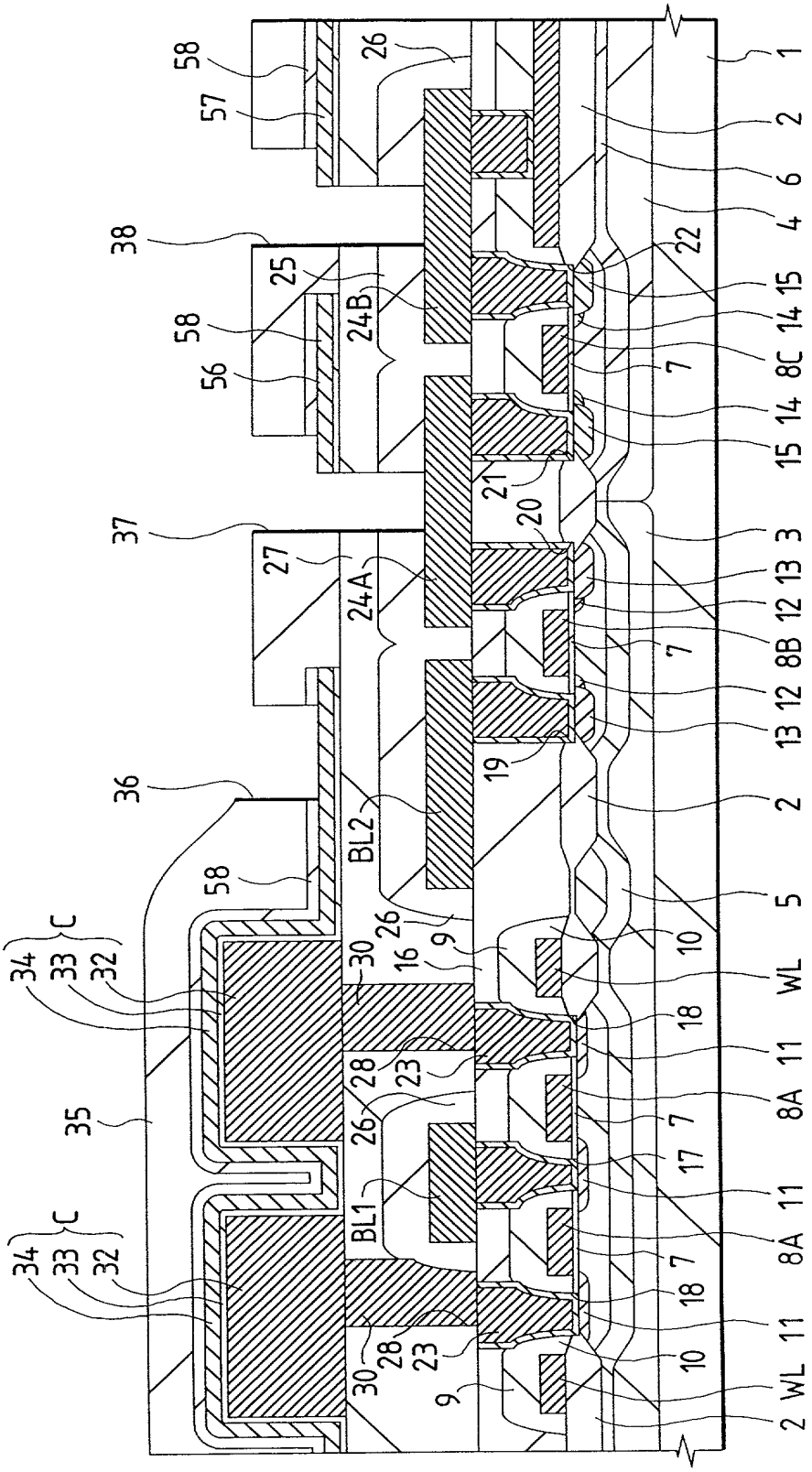

58
57
26
1
38
25
24B
22
2
6
4
58
56
7
15
14
8C
14
15
21
20
37
27
24A
3
13
12
8B
12
13
19
36
BL2
2
58
5
C
34
33
32
26
9
30
16
10
WL
18
11
28
23
8A
35
26
7
17
C
34
33
32
BL1
11
8A
7
18
28
23
10
30
9
WL
2

FIG. 41

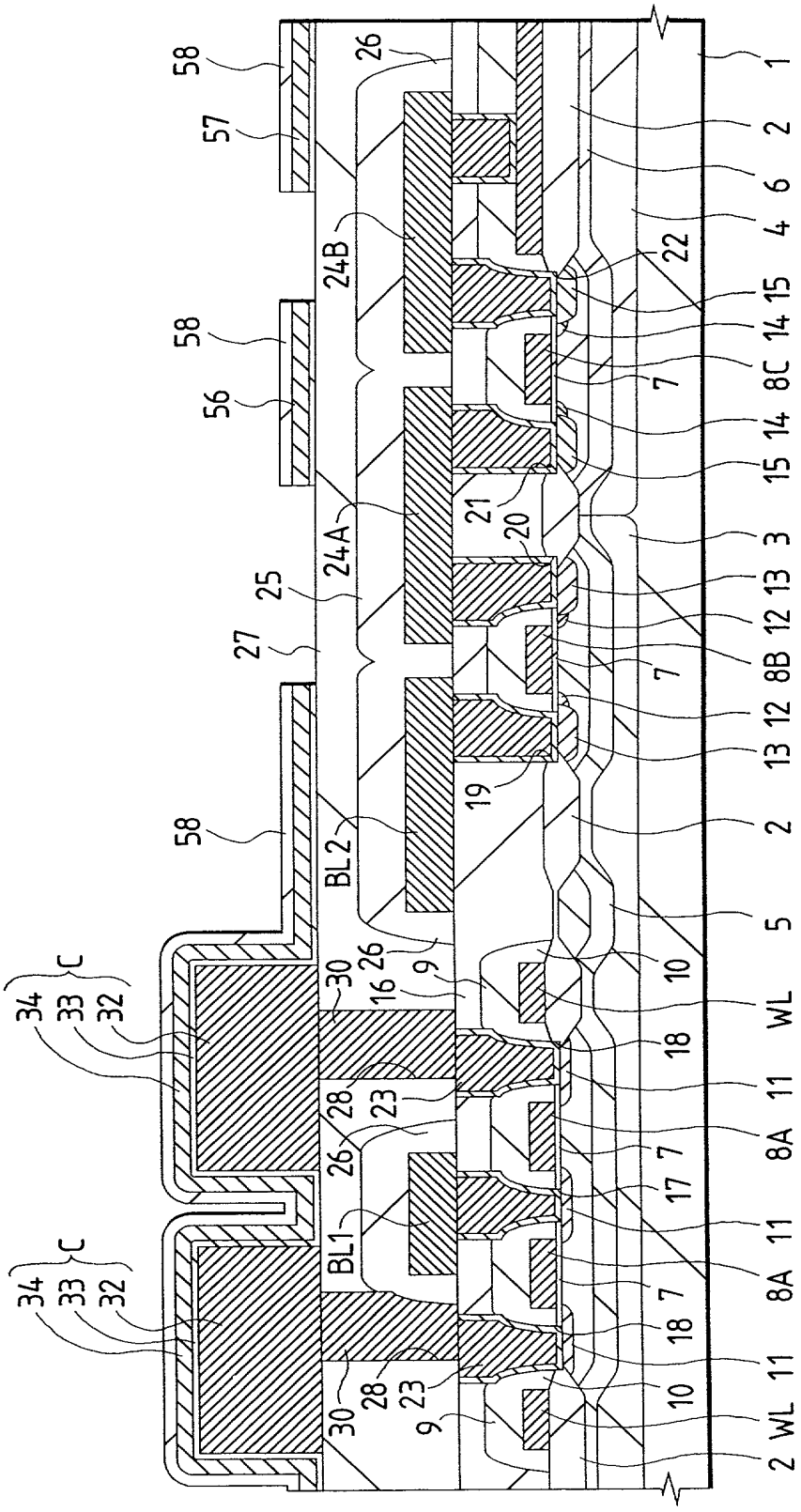
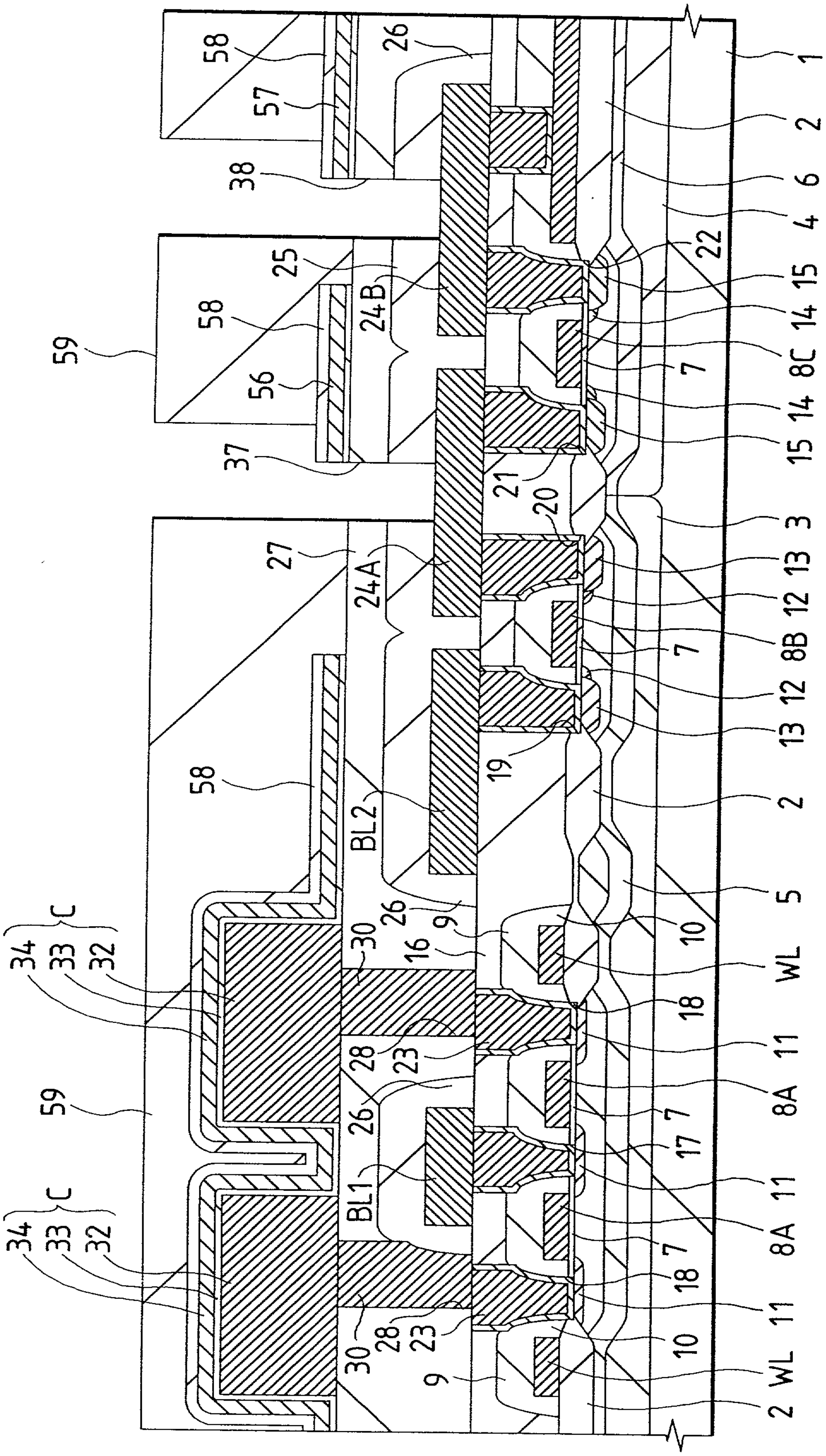

58
57
56
58
58
58
26
24B
24A
25
27
BL2
BL1
34
33
32
C
30
16
26
9
28
23
19
21
20
22
7
1
2
6
4
15
14
8C
14
15
3
13
12
8B
12
13
2
5
10
WL
18
11
8A
11
7
17
11
8A
7
18
10
11
WL
2

FIG. 42


1
2
4
6
22
15
14
8C
7
3
13
12
8B
19
5
10
WL
18
11
8A
17
9
16
20
21
23
24A
24B
25
26
27
28
30
32
33
34
C
37
38
56
57
58
59
BL1
BL2

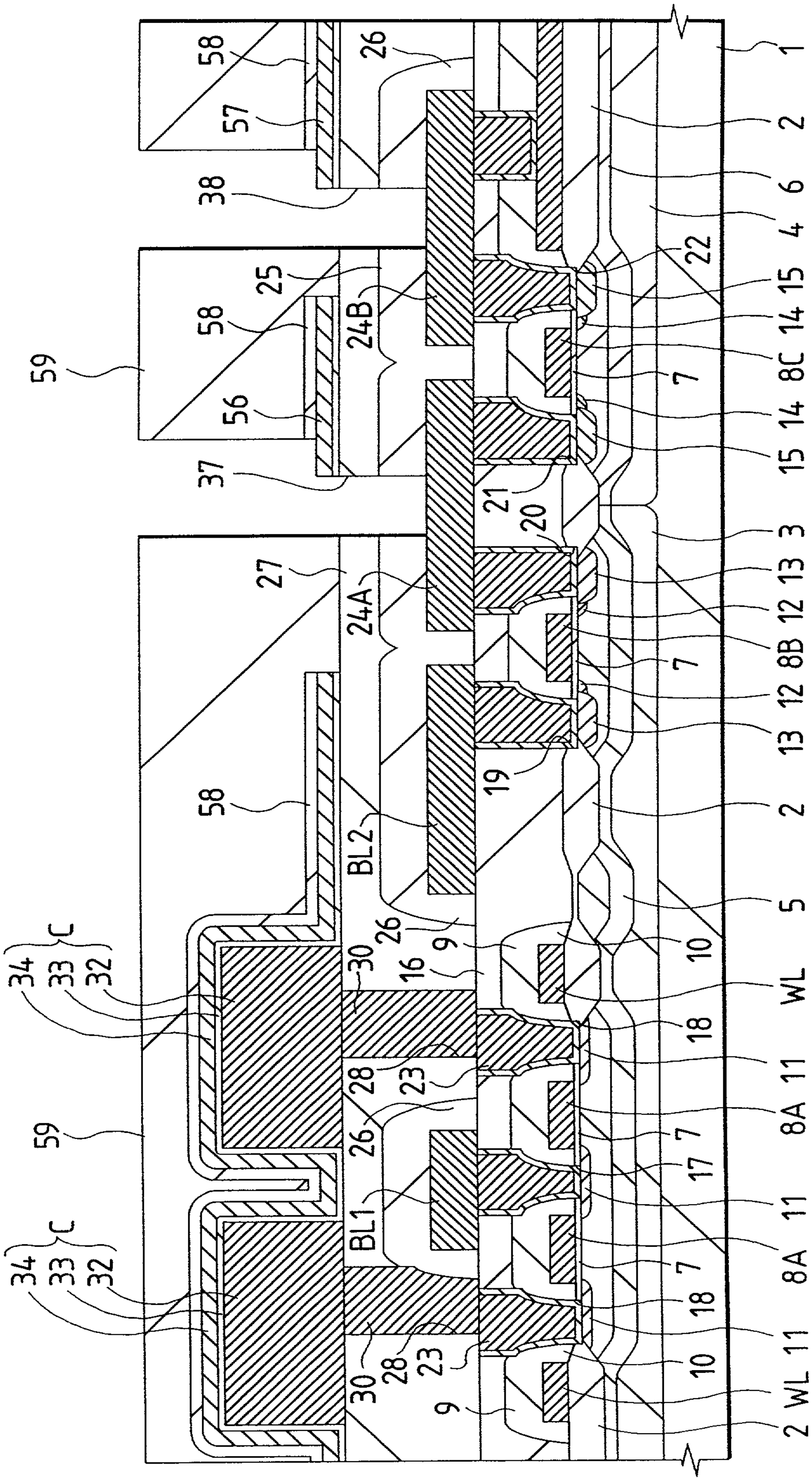

1
2
6
4
22
15
14
8C
7
14
15
3
13
12
8B
7
12
13
2
5
10
WL
18
11
11
8A
7
17
11
8A
7
18
11
10
2 WL
58
57
26
38
59
58
25
24B
56
37
27
24A
21
20
19
58
BL2
26
9
16
30
34
33
32
C
28
23
26
BL1
59
30
28
23
9

FIG. 43

FIG. 44

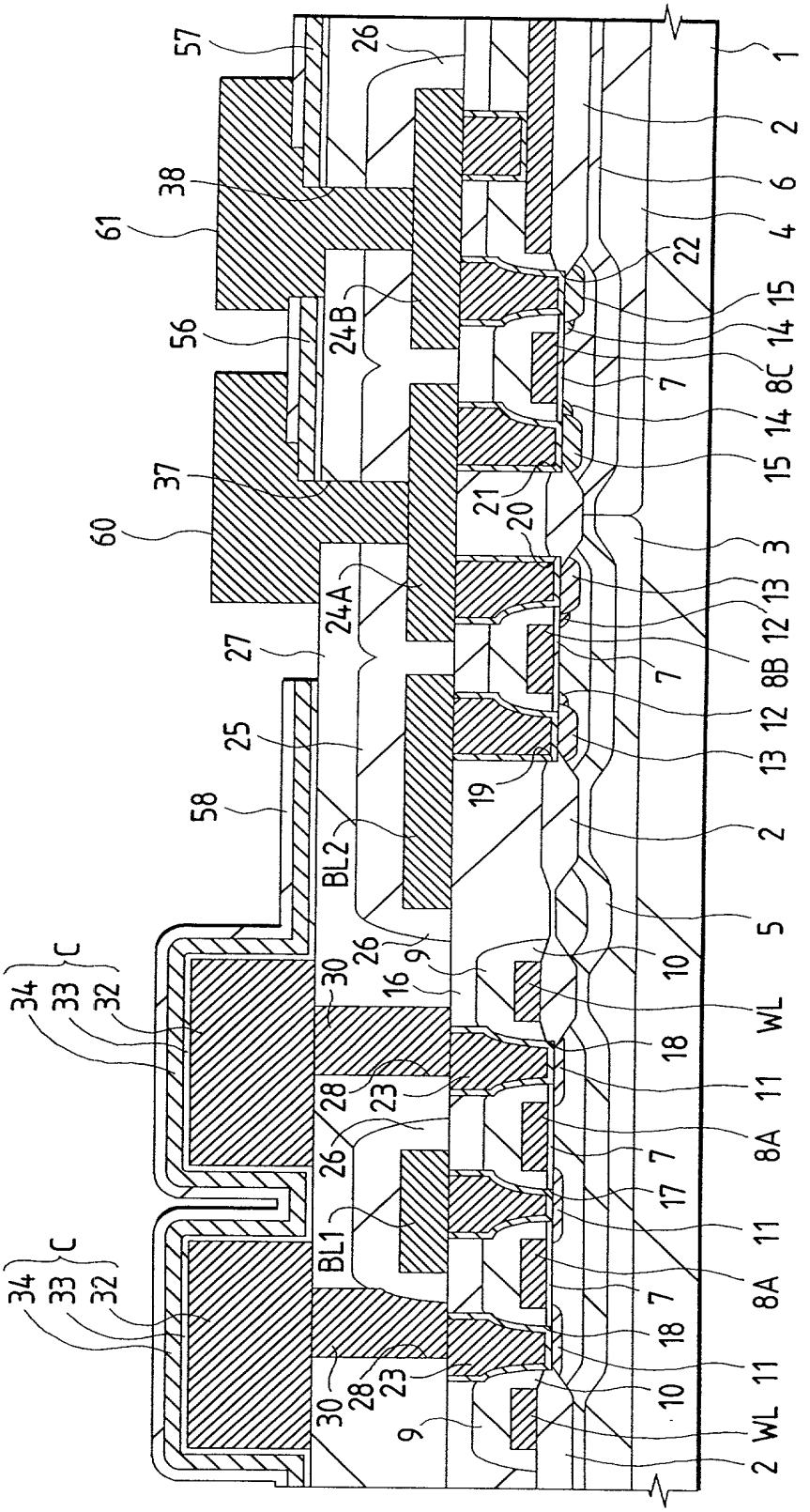

57
26
1
38
2
61
6
4
22
56
24B
15
14
8C
7
37
14
15
21
20
60
3
24A
27
13
12
8B
7
25
12
13
58
19
2
BL2
5
26
9
10
C
34
33
32
30
16
WL
18
28
23
11
26
8A
7
17
BL1
11
C
34
33
32
7
18
28
23
11
30
10
9
WL
2

FIG. 45

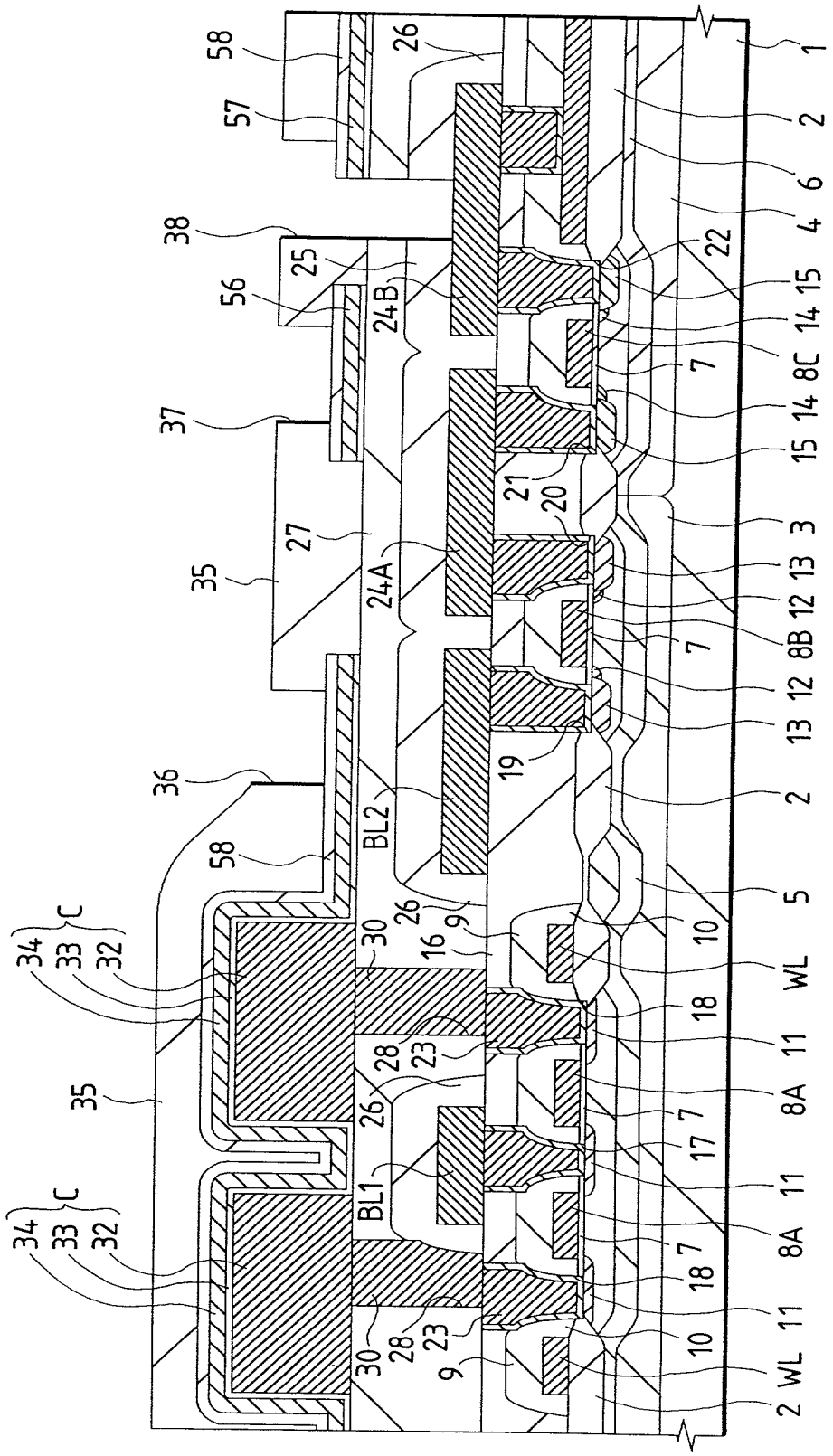

58
57
26
1
2
6
4
38
25
22
56
24B
15
14
7
8C
37
14
15
21
20
27
3
35
24A
13
12
8B
7
12
13
19
36
2
BL2
58
5
34
33
32
C
30
26
9
16
10
WL
18
11
28
23
8A
35
26
7
17
BL1
11
34
33
32
C
8A
7
18
30
28
23
11
10
9
WL
2

FIG. 46

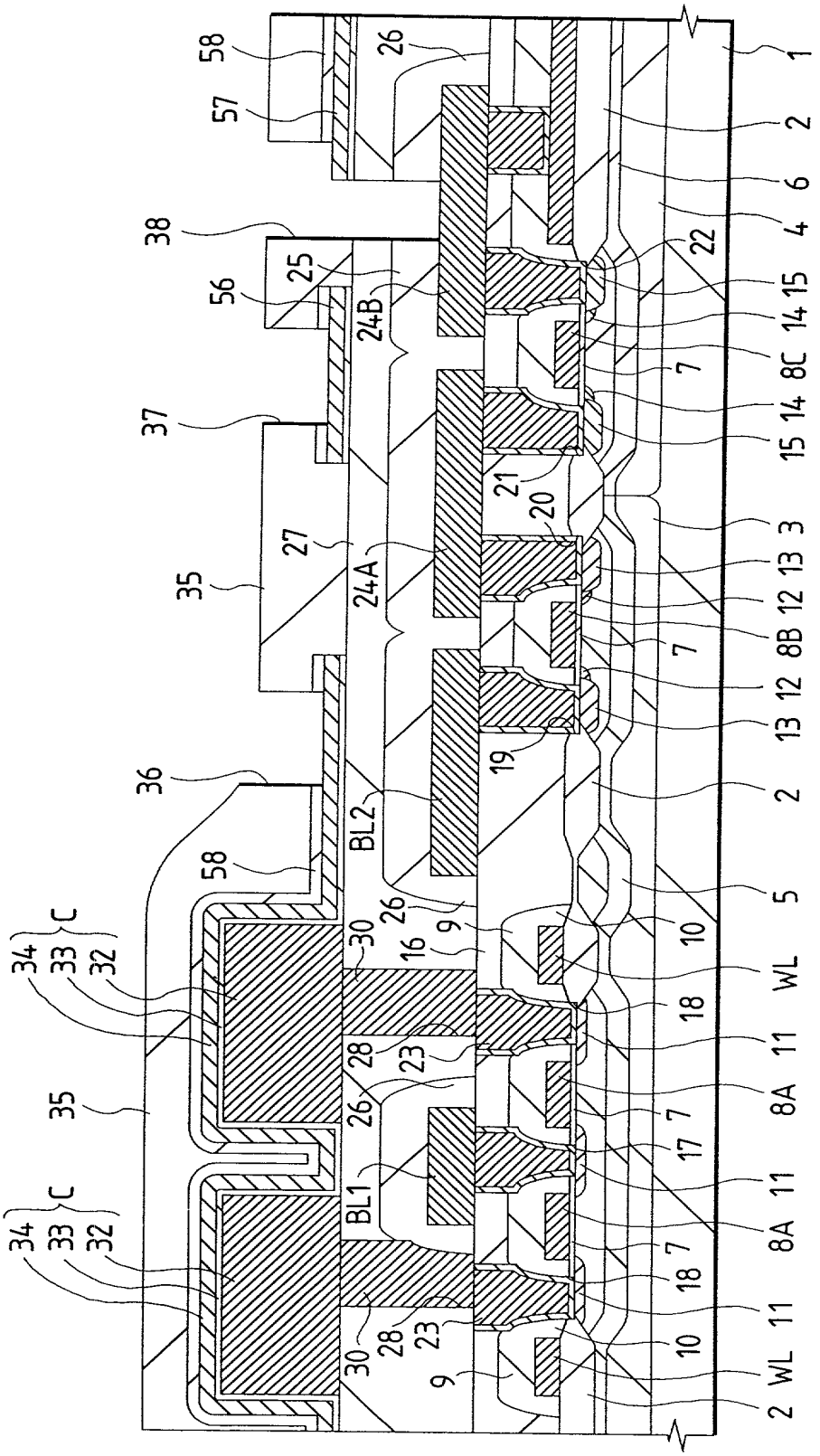

58
57
38
56
37
35
36
34
33
32
C
BL2
BL1
WL
24A
24B
25
26
27
28
30
16
9
23
21
20
19
18
17
10
7
8A
8B
8C
11
12
13
14
15
22
4
6
2
1
3
5

FIG. 47

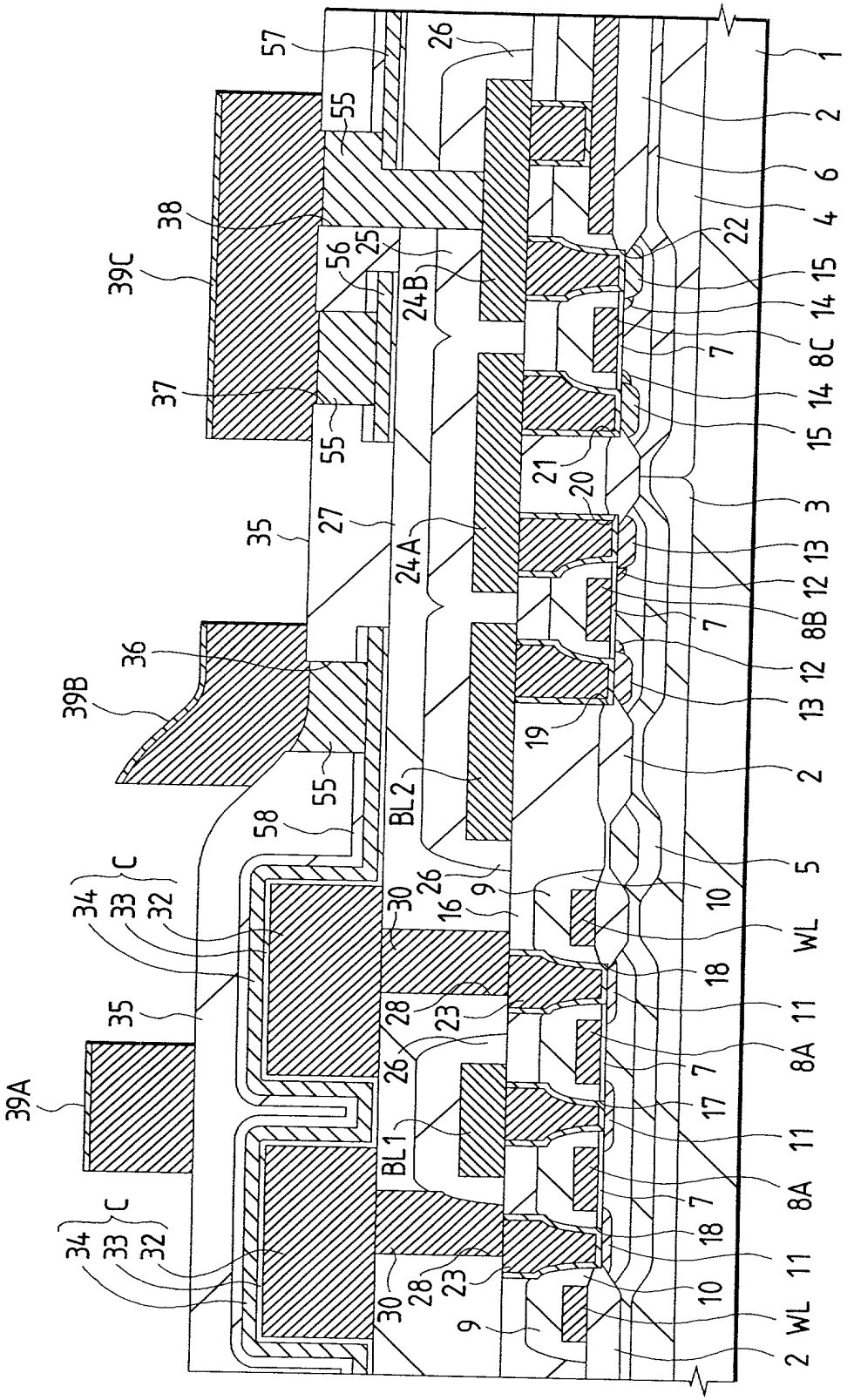

57
55
38
39C
56
25
24B
37
55
35
27
24A
36
39B
55
58
BL2
34
33
32
C
30
26
16
9
35
39A
28
23
26
BL1
34
33
32
C
30
28
23
9
2 WL 11 10 18 7 8A 11 17 7 11 WL 18 11 8A 7 23 28 26 9 10 5 2 13 12 8B 7 13 12 3 15 14 8C 7 14 15 4 6 22 2 1
19
21
20

FIG. 48

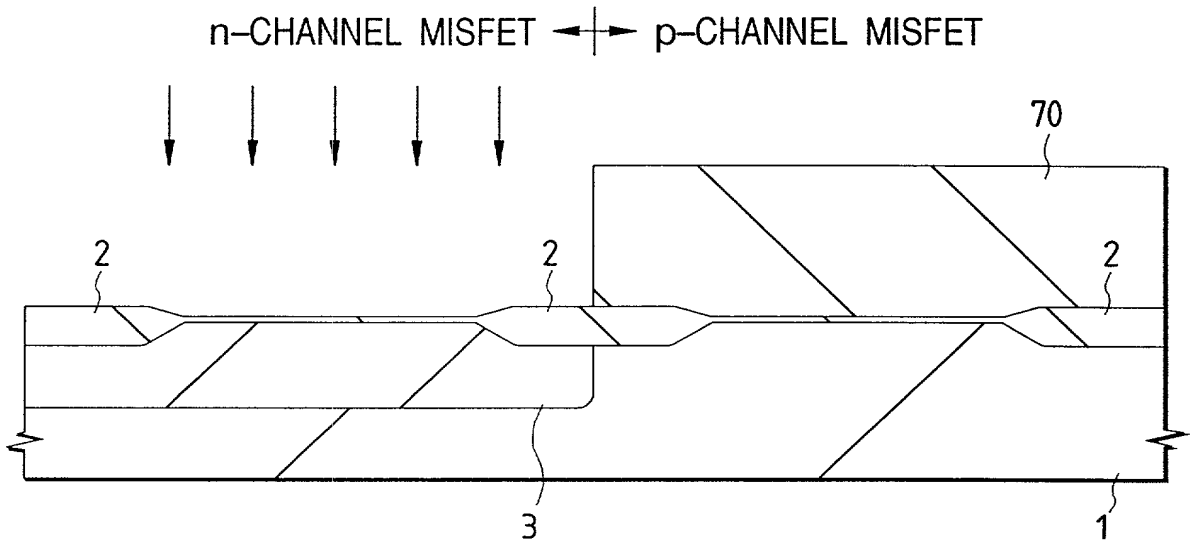


FIG. 49

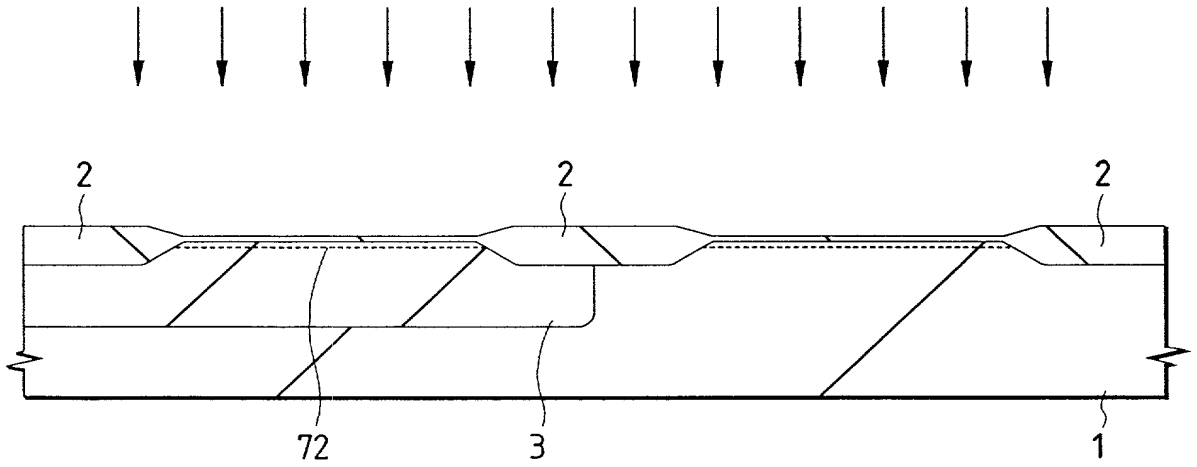


FIG. 50

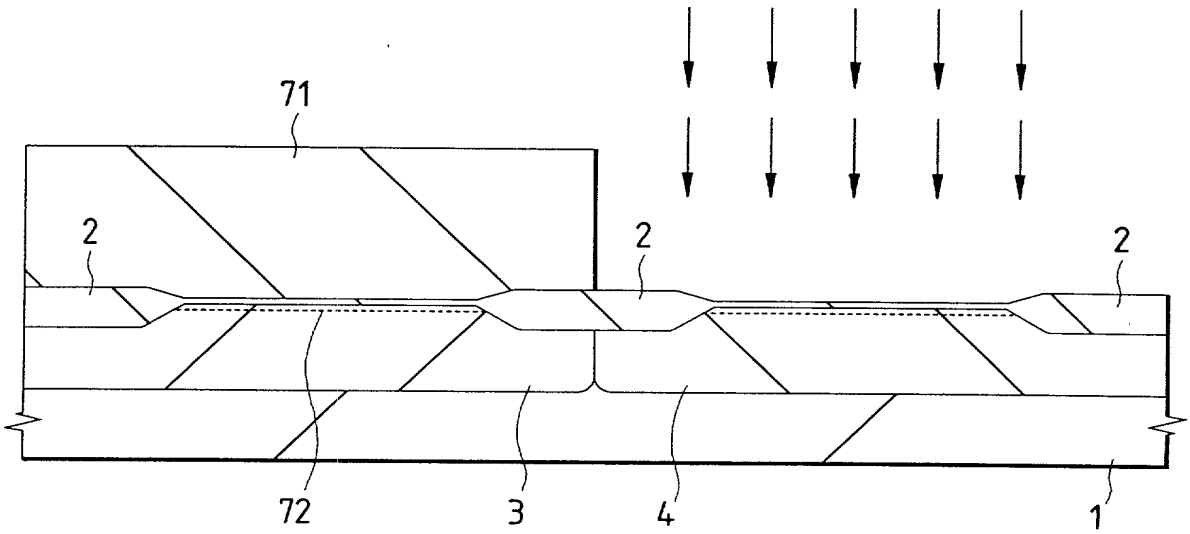


FIG. 51

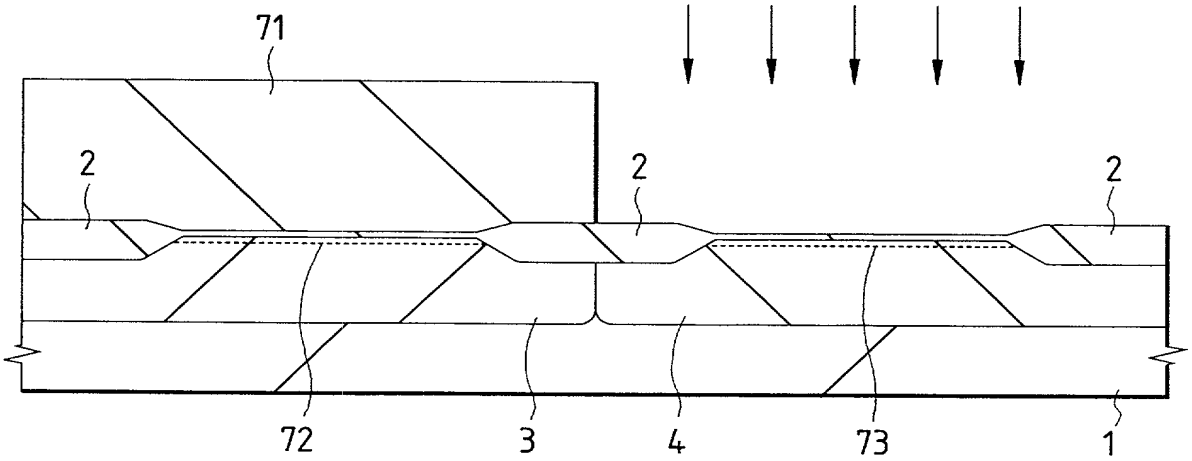


FIG. 52

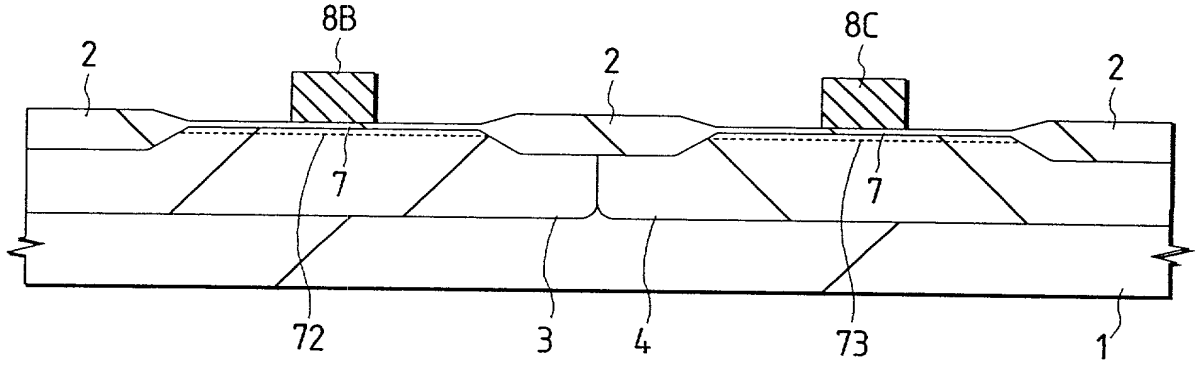

8B
8C
2
2
2
7
7
72
3
4
73
1

FIG. 53

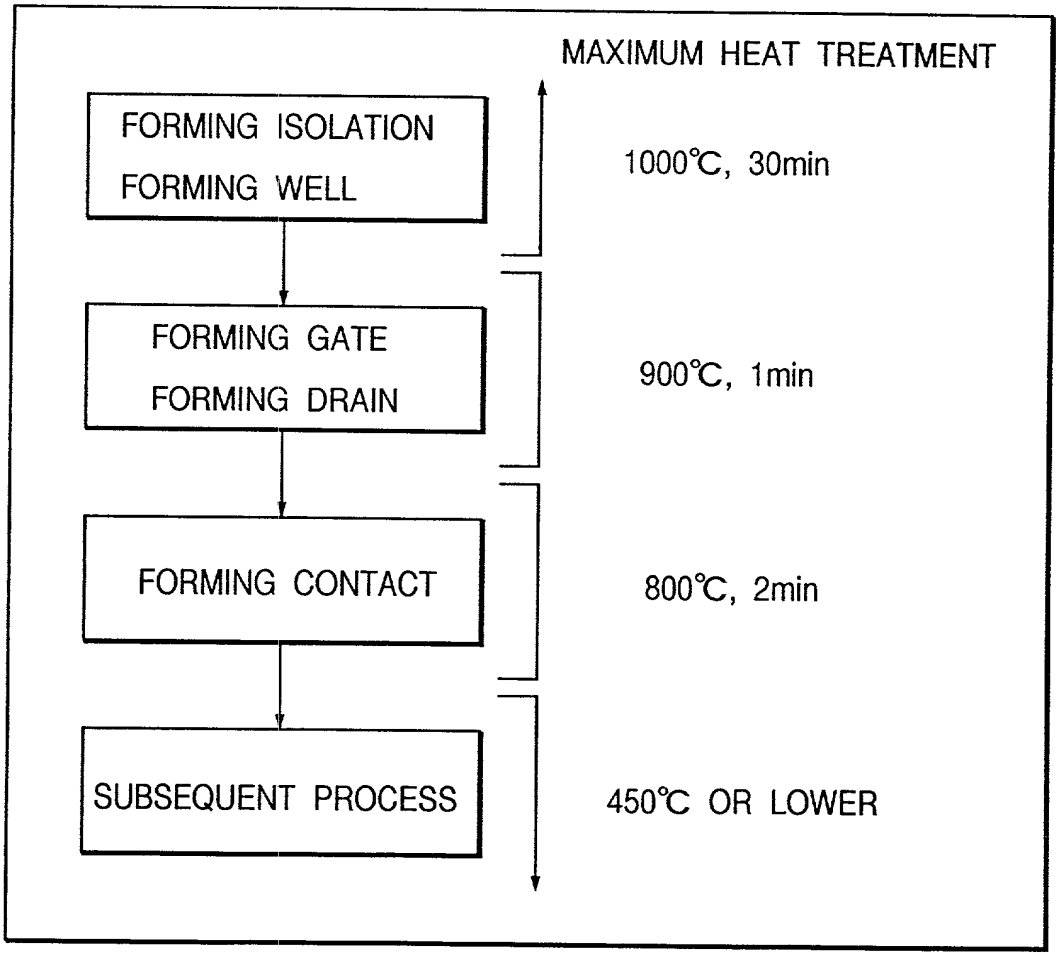

MAXIMUM HEAT TREATMENT
FORMING ISOLATION
FORMING WELL
1000℃, 30min
FORMING GATE
FORMING DRAIN
900℃, 1min
FORMING CONTACT
800℃, 2min
SUBSEQUENT PROCESS
450℃ OR LOWER

FIG. 54

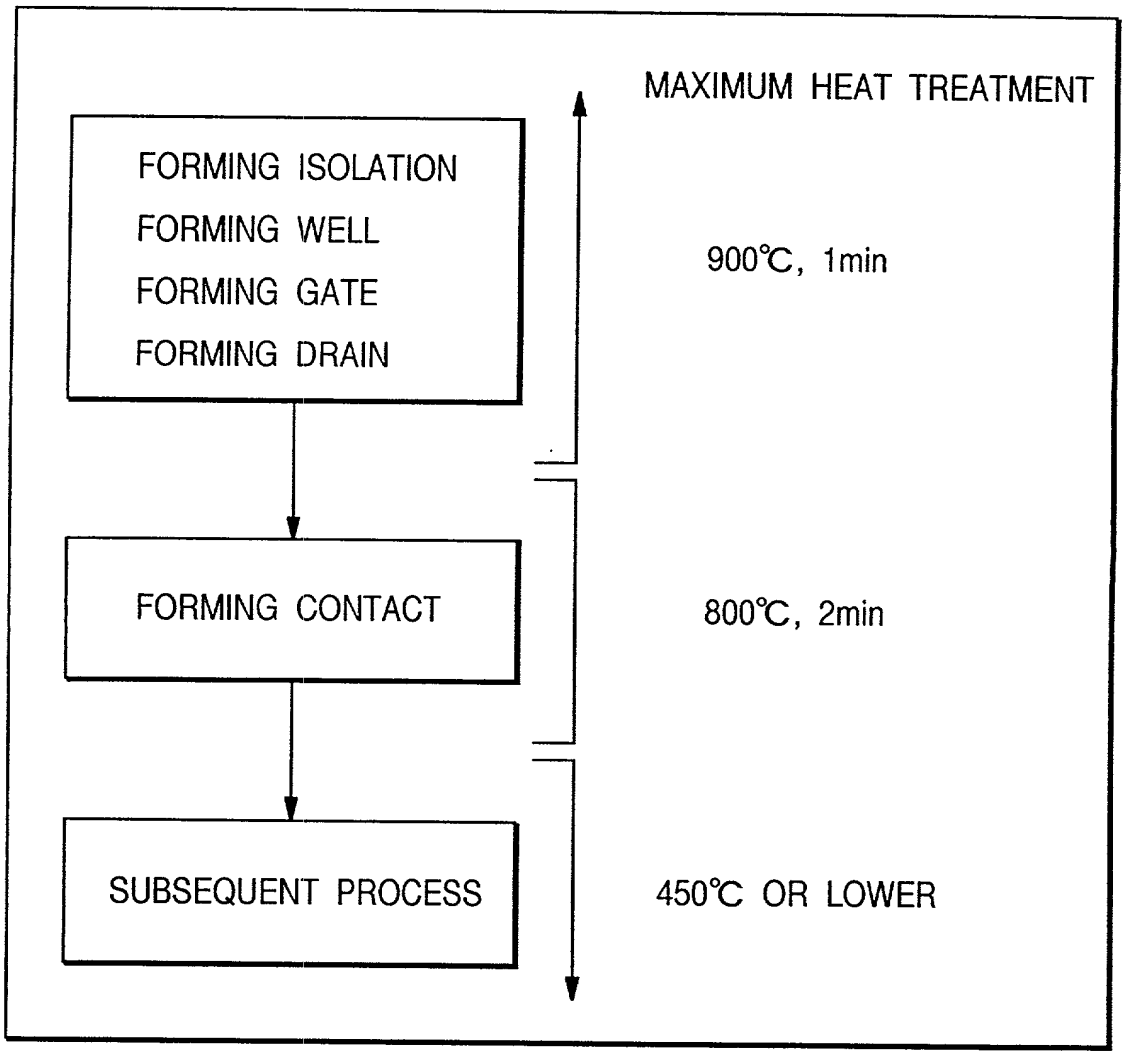

MAXIMUM HEAT TREATMENT
FORMING ISOLATION
FORMING WELL
FORMING GATE
FORMING DRAIN
900℃, 1min
FORMING CONTACT
800℃, 2min
SUBSEQUENT PROCESS
450℃ OR LOWER

FIG. 55

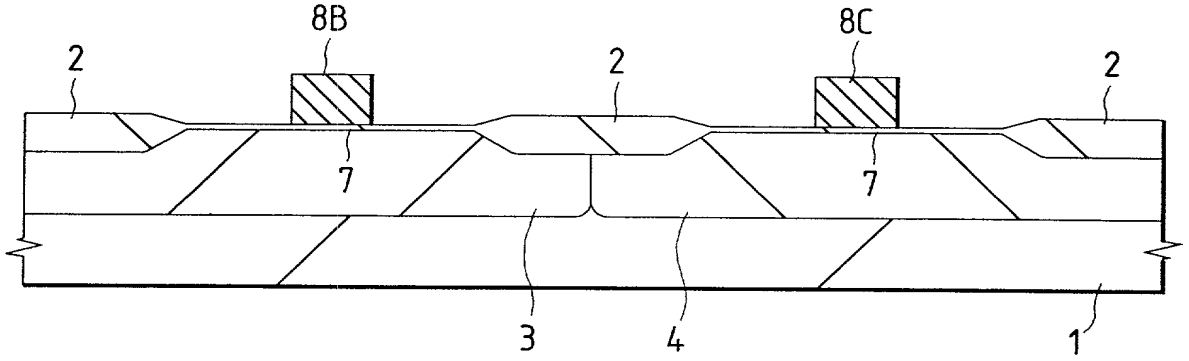


FIG. 56

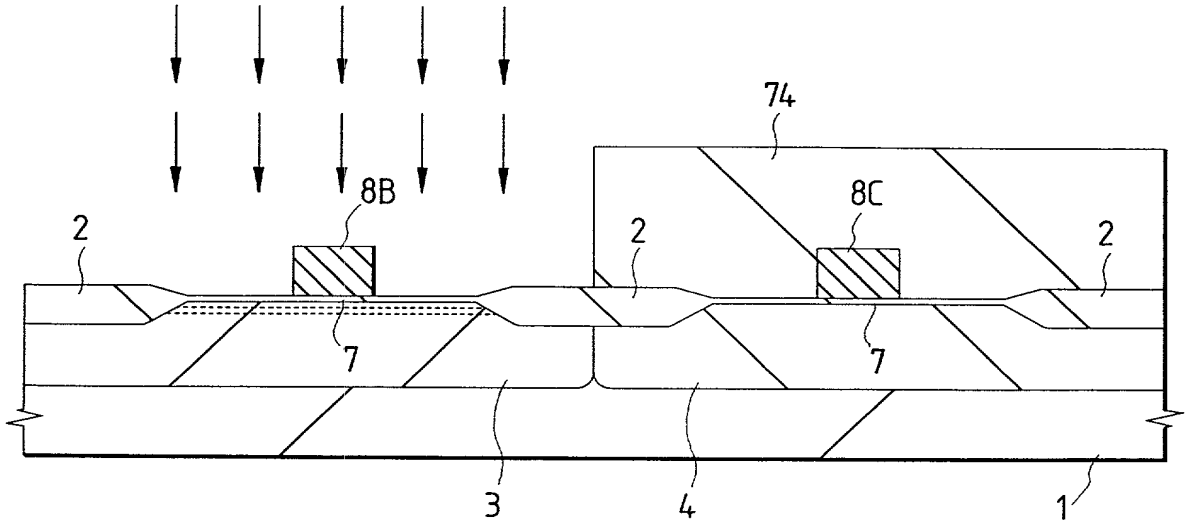


FIG. 57

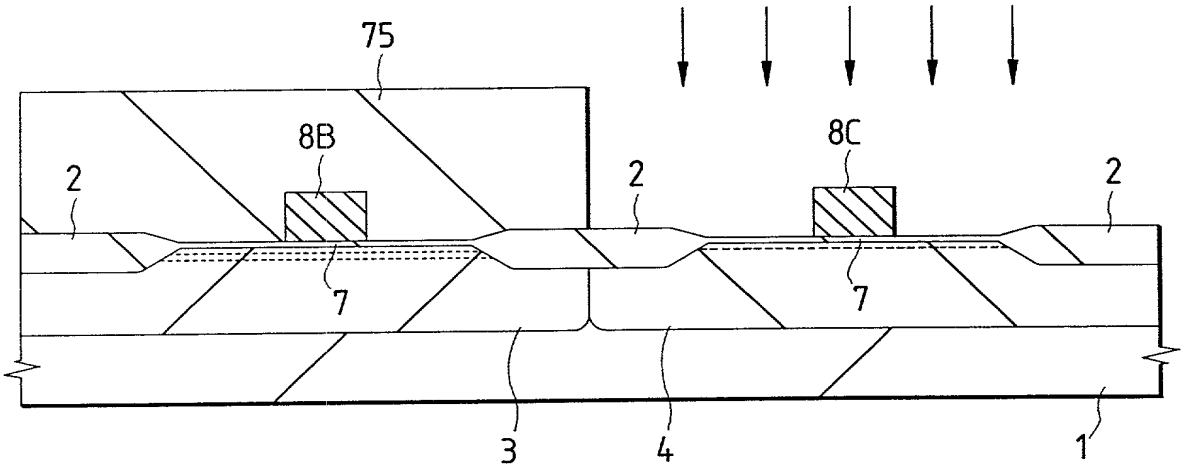
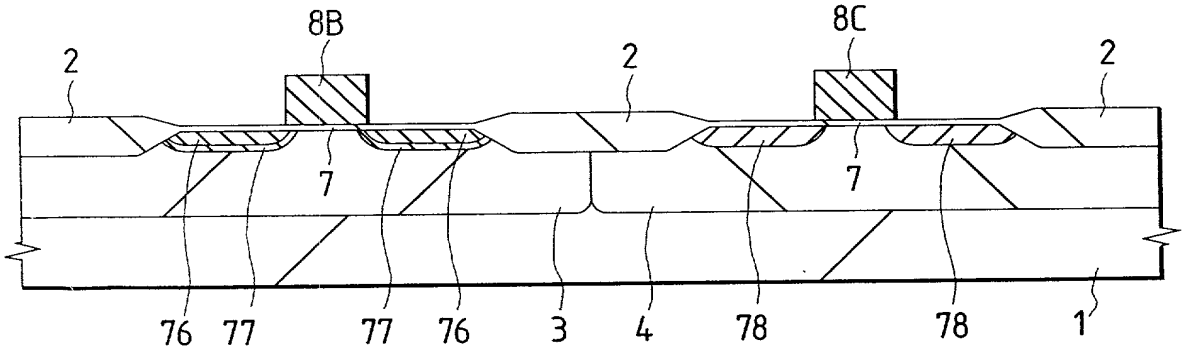


FIG. 58



DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND PROCESS FOR MANUFACTURING THE SAME,

the specification of which (check one)

☐ is attached hereto.

☒ was filed on May 30, 1997
as Application Serial No. _____
and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
8-137957 (Number)	Japan (Country)	31/May/1996 (Day/Month/Year Filed)	☒ Yes	☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes	☐ No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)

(Continued on Page 2)

I hereby appoint as principal attorneys; Donald R. Antonelli, Reg. No. 20,296; David T. Terry, Reg. No. 20,178; Melvin Kraus, Reg. No. 22,466; Stanley A. Wal, Reg. No. 26,432; William I. Solomon, Reg. No. 28,565; Gregory E. Montone, Reg. No. 28,141; Ronald J. Shore, Reg. No. 28,577; Donald E. Stout, Reg. No. 26,422; Alan E. Schiavelli, Reg. No. 32,087; James N. Dresser, Reg. No. 22,973 and Carl I. Brundidge, Reg. No. 29,621 to prosecute and transact all business connected with this application and any related United States application and international applications. Please direct all communications to the following address:

Antonelli, Terry, Stout & Kraus
Suite 1800
1300 North Seventeenth Street
Arlington, Virginia 22209
Telephone: (703) 312-6600
Fax: (703) 312-6666

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United State Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

(Full Name) (Signature)

Date June 10, 1997 Inventor Makoto YOSHIDA Makoto Yoshida
Residence Same as Post Office Address Citizenship Japan
Post Office Address 769, Shin-machi, Ome-shi, Tokyo, Japan

Date June 10, 1997 Inventor Takahiro KUMAUCHI Takahiro Kumauchi
Residence Same as Post Office Address Citizenship Japan
Post Office Address 2-1-16-A-105, Midorigaoka, Hamura-shi, Tokyo, Japan

Date June 10, 1997 Inventor Yoshitaka TADAKI Yoshitaka Tadaki
Residence Same as Post Office Address Citizenship Japan
Post Office Address 4-6-18, Misugidai, Hannou-shi, Saitama, Japan

Date June 10, 1997 Inventor Kazuhiko KAJIGAYA Kazuhiko Kajigaya
Residence Same as Post Office Address Citizenship Japan
Post Office Address 905-6, Shimoyaganuki, Iruma-shi, Saitama, Japan

Date June 10, 1997 Inventor Hideo AOKI Hideo Aoki
Residence Same as Post Office Address Citizenship Japan
Post Office Address 1-7-3-302, Ozakudai, Hamura-shi, Tokyo, Japan

Date June 10, 1997 Inventor Isamu ASANO Isamu Asano
Residence Same as Post Office Address Citizenship Japan
Post Office Address 1314-3-804, Shimofujisawa, Iruma-shi, Saitama, Japan

Date _____ Inventor _____
Residence _____ Citizenship _____
Post Office Address _____

Date _____ Inventor _____
Residence _____ Citizenship _____
Post Office Address _____

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Residence _____ Citizenship _____
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